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USE **REINFORCED ISOLATION** FOR EFFECTIVE DATA COUPLERS

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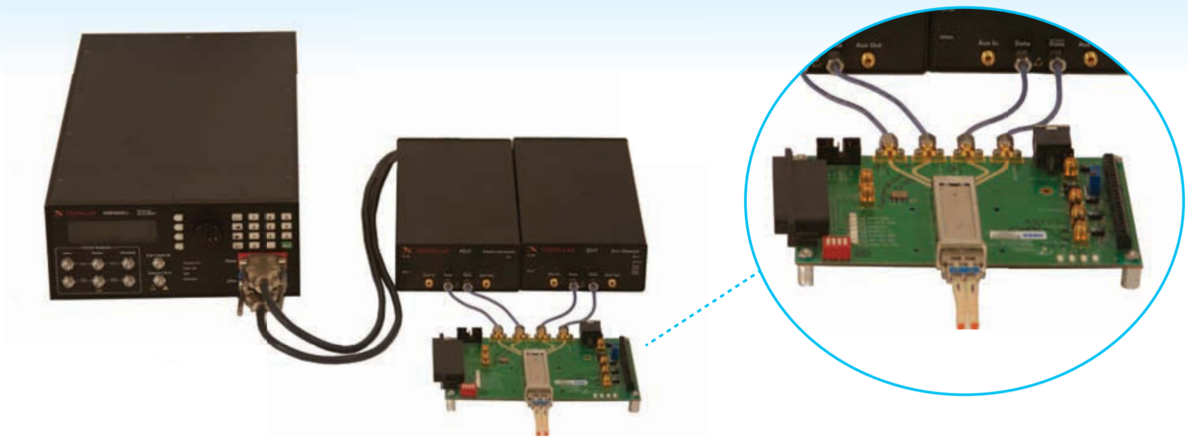

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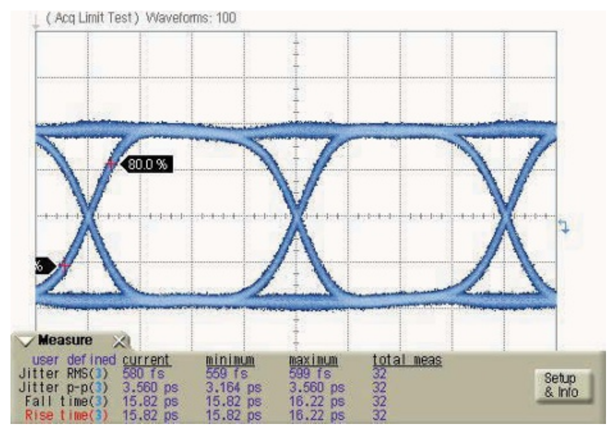

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How to pick the perfect inductor for your LED driver application

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Or evaluate newer, high performance parts that weren't available when the reference design was created?

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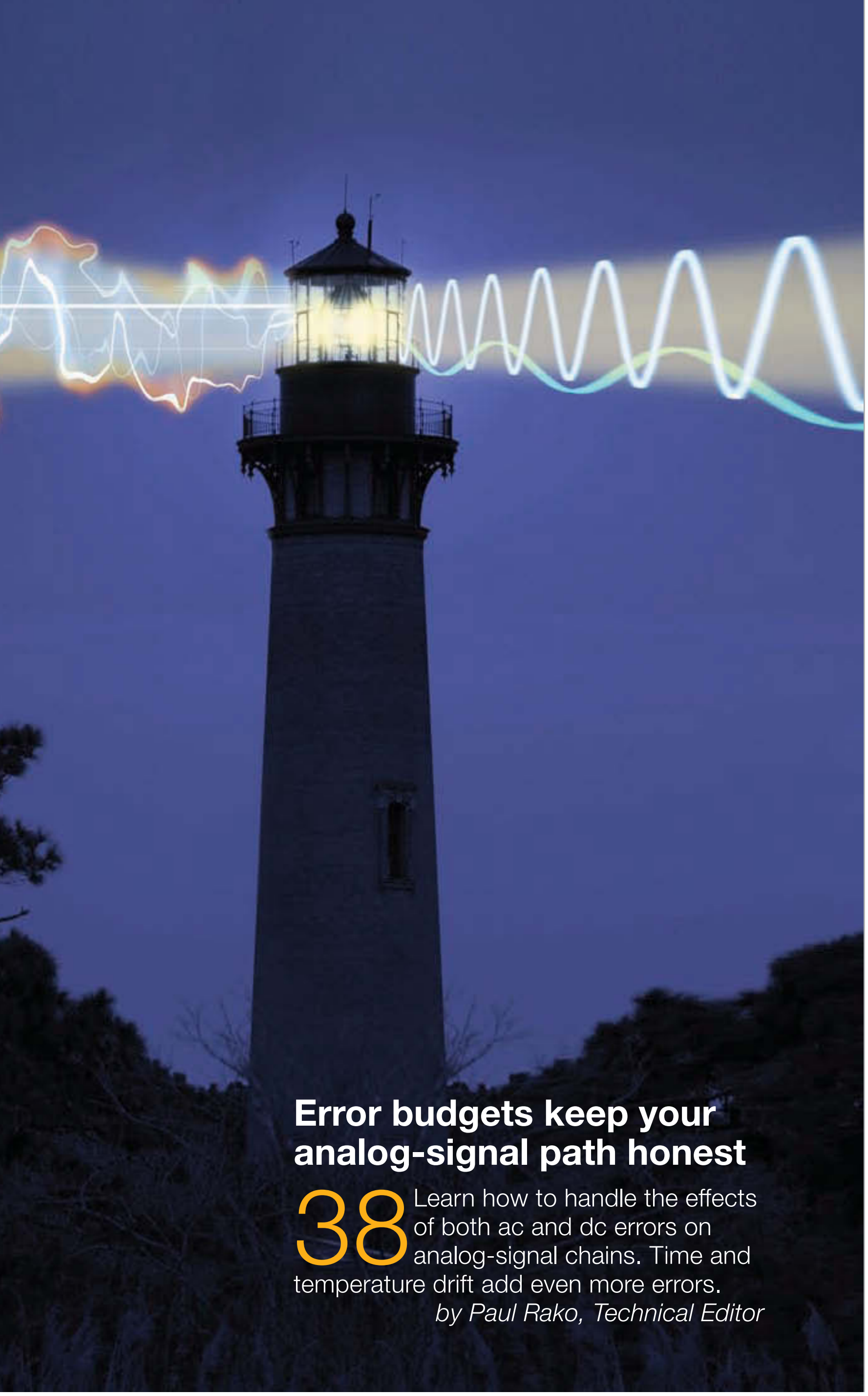

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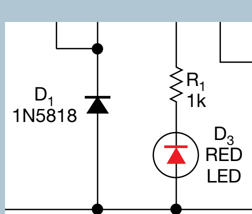
DESIGNIDEAS



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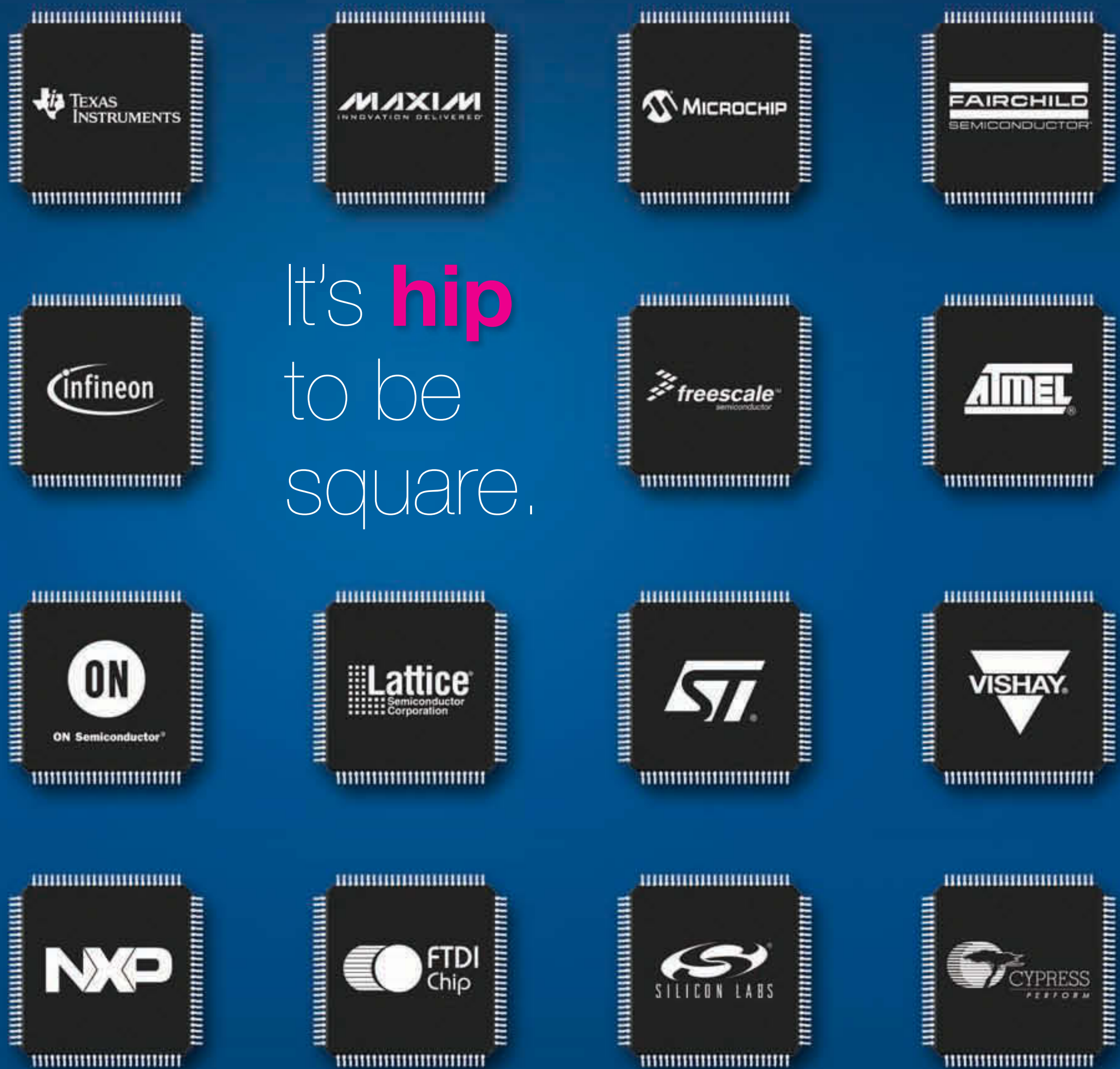

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pulse

DEPARTMENTS & COLUMNS

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Volume 56, Number 20 (Printed in USA).

Benchmark MOSFETs

DC-DC Buck Converter and POL Applications

SO-8

Part	V	nC	mΩ
IRF8788PBF	30	44	2.8
IRF8714PBF (Ctrl)	30	8.1	8.7
IRF7862PBF (Sync)	30	30	3.7

PQFN (5x6)

Part	V	nC	mΩ
IRFH5303	30	15	4.2
IRFH5304	30	16	4.5
IRFH5306	30	7.8	8.1
IRFH5301	30	37	1.9
IRFH5302	30	4.8	2.1
IRFH5302D	30	26	2.5

PQFN (3x3)

Part	V	nC	mΩ
IRFHM831	30	7.3	7.8
IRFHM830	30	15	3.8
IRFHM830D	30	13	4.3

PQFN (2x2)

Part	V	nC	mΩ
IRFHS8342	30	4.2	16
IRFHS8242	25	4.3	13

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JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN*'s community

In response to "Buyers of electric vehicles (EVs) may be very disappointed," posted in Patrick Mannion's Design Cycle blog at http://bit.ly/nyLSTu, Watashi commented:

"When ultra-capacitors and high-temperature superconductor motors sell for the same (or slightly higher) price point as batteries and conventional motors, EVs may be acceptable to the market. Cost/benefit ratios are what drive human nature, and unfortunately, EVs suffer tremendously in that arena."

In response to "Hackers liberate intelligent Christmas lights," posted in Margery Conner's PowerSource blog at http://bit.ly/q2OeYl, William Ketel commented:

"While it is possible that the LED portion will last that long ... there are a lot of much weaker links in the chain that will fail far sooner. ... After all, the primary design target of any consumer good is minimum cost to produce. That is also the secondary design target. I am not aware of durability being on the list, even. So what becomes of all those Internet addresses after the part fails? Has anybody ever thought of that?"

In response to "Doing too much at once?" posted in Brian Bailey's Practical Chip Design blog at http://bit.ly/npbJg9, Andy T commented:

"Hiding features is fine, but I still want access to ALL of the hardware with an 'unhide' in the event I need, or want, to get clever with the capability of the device at the configuration bit level—an unforeseen (by 'them') or proprietary (my) capability. FPGA vendors are among the worst for this FOS (fear of support). Having worked for one, I know what was in the chip and what was not 'allowed' for customers to access."

***EDN* invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post. To review current comment threads on EDN.com, visit http://bit.ly/EDN_Talkback.**

CONTENT

Can't-miss content on EDN.com

A PRACTICAL APPROACH TO IP-QUALITY INSPECTION

A robust process that can automatically assess IP quality at incoming inspection can have a large impact on your schedule and overall well-being.

http://bit.ly/pW1MOv

CREE TAKES A PAGE FROM AMAZON'S PLAYBOOK WITH ITS NEW LED TEMPO SERVICE

Jeff Bezos, head of Amazon, has been quoted as saying, "There are two ways to build a product. The first: a company starts with their strengths and builds to the needs of the consumer. The second: a company starts with the needs of the consumer and builds [into] the strengths of the company." Like Amazon, Cree is another rare company that does both.

http://bit.ly/pRZB4I

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Opportunities to get involved and show your smarts

ARM TechCon—http://bit.ly/EDN_ARMTechCon

The event, which starts October 25, aims to connect, instruct, advise, and enable the world of electronic and computer design. This year's technical conference offers two distinct elements: Chip Design Day, a one-day intensive conference for chip-design teams working with ARM silicon IP and tools; and Software and Systems Design Days, two days geared toward those interested in building ARM-based modules, boards, and systems.

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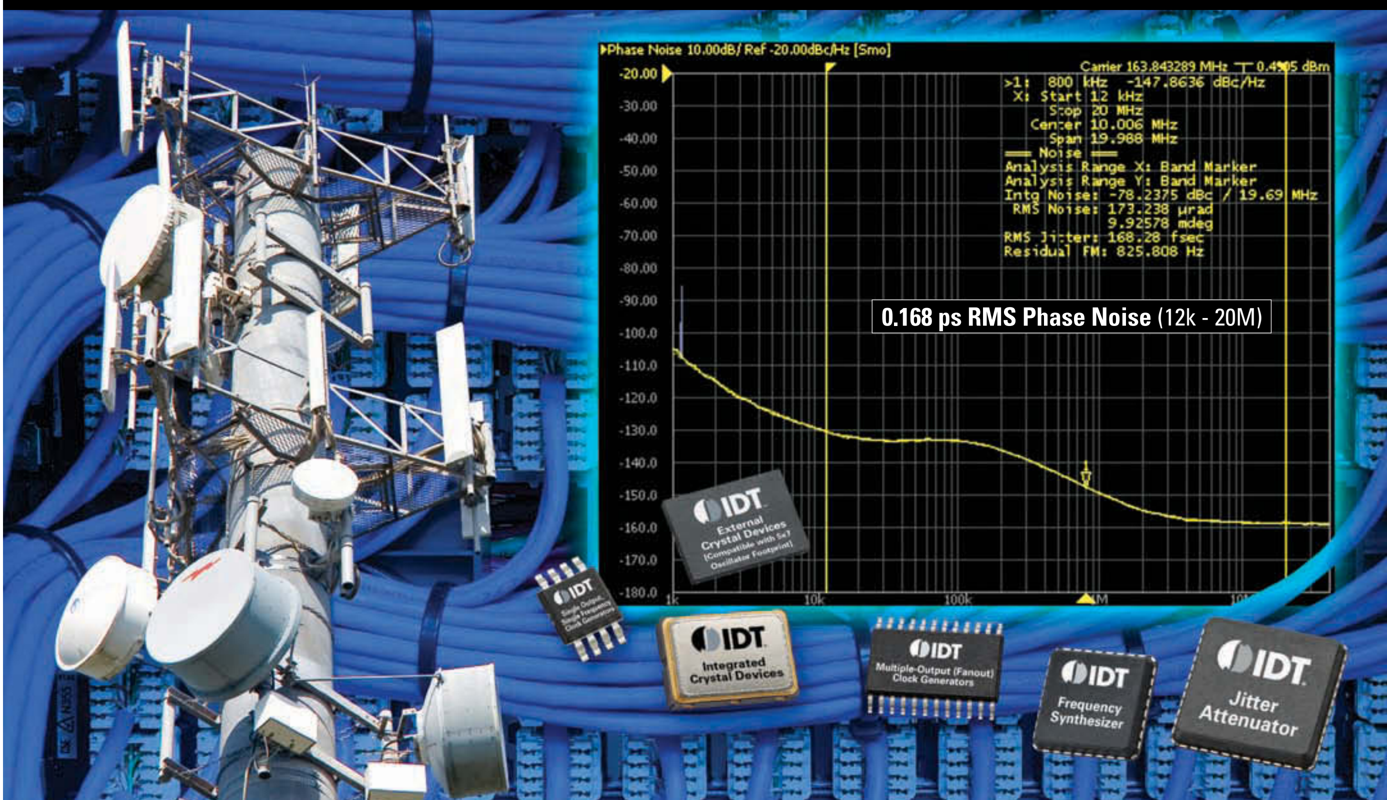
From *EDN*

Additional comments here: "Steve Jobs life lessons," http://bit.ly/EDN_SteveJobs

Integrated Device Technology FemtoClock NG – When a Trillionth Of a Second is Just Too Long



The FemtoClock Next Generation (NG) clock synthesiser family allows engineers to generate almost any output frequency from a fixed frequency crystal, and to meet the challenges of the most demanding timing applications.

Use of a single source to generate multiple clocks often leads to increased susceptibility to power supply noise and restrictions on multiplication factors. IDT's technology effectively eliminates these problems by doubling the power-supply noise rejection (PSNR) of previous generation devices while also introducing the potential for virtually limitless customization of output frequency.

An innovative fractional multiplier PLL architecture introduces the flexibility for engineers to generate any output frequency from any input frequency. And the advanced design of the FemtoClock NG family achieves greater than 80 dB of PSNR to make the devices immune to power-supply noise.

Other performance benefits of FemtoClock NG technology include low power consumption and a clocking performance of under 0.5 ps RMS phase noise jitter! The devices offer standard outputs such as differential LVPECL, LVDS and single-ended LVCMOS, providing a precise fit to any application.

With FemtoClock NG technology, IDT has eliminated the most challenging aspects of silicon-based clock design and introduced an unprecedented level of flexibility for clocking in high-performance applications.

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FSW analyzer shows multiple measurements in single window

Rohde & Schwarz's new FSW signal and spectrum analyzer comes in three models that cover 2 Hz to 8, 13, or 26.5 GHz and comes in 80- and 160-MHz-bandwidth versions. As the eventual replacement for the FSU spectrum analyzer and the FSQ signal analyzer, the FSW targets use in development laboratories in aerospace, defense, and communications. The FSU has a 20-Hz to 67-GHz frequency, and the FSQ has a 120-MHz bandwidth and a 20-Hz to 40-GHz frequency. Those units will remain in production for two to three years, and the FSW's specification will expand to match its predecessors' bandwidth and frequency.

A 12.1-in. touchscreen enables a multiview function to simultaneously display the results of multiple applications and eliminates time-consuming switching between the applications. At a 10-kHz carrier offset, the FSW achieves a phase-noise specification of less than –137 dBc at 1 Hz, which is as much as 10 dB less than comparable instruments. This spec is important for developers of RF components and complete systems for radar applications.

With the optional FSW-K6, the FSW also supports analysis of pulsed signals. It allows the unit to measure wideband, hopping, and chirp signals for wireless standards, such as 802.11ac. The FSW also enables developers to quickly detect spurious emissions.

The FSW can optionally include FSW-B13 switchable highpass filters for carrier frequencies as high as 1.5 GHz for harmonic measurements on transmitter systems, resulting in improved dynamic range over conventional spectrum analyzers and eliminating the need for external filters. This feature facilitates test-system setup for GSM (global-system-for-mobile)-communication, CDMA (code-division-multiple-access), WCDMA (wide-band-CDMA), LTE (long-term-evolution), and TETRA (terrestrial-trunked-radio) systems, for example.

The company's Legacy Pro technology enables the FSW to support the remote-control command sets of Rohde & Schwarz and other vendors' instruments. Users can exchange the FSW's internal solid-state disk for a neutral solid-state disk and can send their instruments for calibration without having any confidential test data leave the lab. Device-specific alignment data remains in the analyzer, separate from the user data.

—by Colin Holland

▷**Rohde & Schwarz,**
www.rohde-schwarz.com.

The FSW analyzer has a 12.1-in. touchscreen, enabling a multiview function to simultaneously display the results of multiple applications.

"As a consumer, my main concern ... about modern gadgetry is that so often ... [its] accompanying sophistication makes it unreliable! Instead of a KISS [keep it simple, stupid] philosophy, they put in frilly features, peripheral to the product's main intended function, and it tends to [wear out] first and make the whole widget irreparable and disposable."

—Reader "Frank," in *EDN*'s Talkback section, at http://bit.ly/pTtg4F. Add your comments.

ST adds Cortex-M4 devices to STM32 portfolio

STMicroelectronics based its new STM32 F4 series of microcontrollers on the ARM Cortex-M4 core, which adds signal-processing capabilities and faster operations. The STM32 F4 series extends the STM32 portfolio and has more than 250 compatible devices in production, including the F1 series, the F2 series, and the ultra-low-power L1 series. The company is widening its target applications with the STM32 F4 series. Its single-cycle DSP instructions should provide access to the DSC (digital-signal-controller) market, which requires high computational capability and DSP instructions for applications such as high-end motor control, medical equipment, and security.

The F4 series provides a pin- and software-compatible upgrade from the STM32 F2 series with more SRAM; higher performance; and peripherals for imaging, connectivity, and encryption. The F4 series operates at 168 MHz compared with 120 MHz for the F2 and provides single-cycle DSP-instruction support and an FPU (floating-point unit), 192 kbytes of SRAM compared with 128 kbytes for the F2, and 512 kbytes to 1 Mbyte of embedded flash memory.

The F4 series provides ultra-fast data transfers, with a seven-layer, multiple-AHB (advanced high-performance-bus) matrix and multiple DMA (direct-memory-access) controllers, which allow concurrent execution and data transfers. The integrated single-precision FPU boosts the execution of control algorithms, improves code efficiency, eliminates scaling and saturation, and allows the use of meta-language tools.

The device integrates a reset circuit, PLLs (phase-locked loops), and a less-than-1-μA real-time clock with less-than-1-sec accuracy. It has 4 kbytes of backup SRAM to save data in standby or battery-backup mode. Typical real-time-clock power consumption is less than 1 μA in battery-voltage mode, and an internal voltage regulator with power scaling enables the trade-off of performance versus power consumption.

Connectivity includes a camera interface; a cryptography/hash-encryption hardware processor; a 10- and 100-GbE (gigabit-Ethernet) MAC (media-access controller) with IEEE 1588 Version 2 support; and two USB (Universal Serial Bus) OTG (On-The-Go) ports, one of which has HS (high-speed) support.

The device includes a dedicated audio PLL and two full-duplex I²S (inter-integrated-circuit-sound) ports. It also has as many as 15 communication interfaces, including six USARTs (universal synchronous/asynchronous receivers/transmitters) operating as fast as 10.5 Mbps, three SPIs (serial-peripheral interfaces) operating as fast as 42 Mbps, three I²C (inter-integrated-circuit) ports, two CAN (controller-area-network) interfaces, and one SDIO (serial-digital input/output) interface. The analog circuits include two 12-bit DACs; three 12-bit ADCs with rates as high as 2.4M or 7.2M samples/sec in interleaved mode; and as many as 17 timers, including 16- and 32-bit devices operating as fast as 168 MHz.

The F4 series of microcontrollers provides a pin- and software-compatible upgrade from the STM32 F2 series with more SRAM; higher performance; and peripherals for imaging, connectivity, and encryption.

Four variants are available. The STM32F405x has timers, three ADCs, two DACs, serial interfaces, an external memory interface, a real-time clock, a CRC (cyclic-redundancy-check)-calculation unit, and an analog true-random-number generator, as well as a USB OTG FS (full-speed)/HS interface. It is available in WLCSP64, LQFP64, LQFP100, and LQFP144 packages with 1 Mbyte of flash.

STM32F407 products add a second FS-only USB OTG interface; an integrated 10- and 100-GbE MAC supporting both an MII (media-independent interface) and an RMII (reduced-media-independent interface), with IEEE-1588 precise-time protocol Version 2 hardware support and an 8- to 14-bit parallel camera interface allowing the connection of a CMOS camera sensor that supports speeds as high as 67.2 Mbytes/sec. Devices are available in LQFP100, LQFP144, and LQFP/BGA176 packages, with 512 kbytes to 1 Mbyte of flash.

The STM32F415 and STM32F417 parts add a cryptography/hash-encryption processor to the STM32F405 and STM32F407. The processor has hardware acceleration for AES (Advanced Encryption Standard) 128, 192, and 256; Triple DES (Data Encryption Standard); the MD5 (Message Digest 5) algorithm; and the SHA-1 (Secure Hashing Algorithm-1). The devices are in volume production, and prices begin at $5.74 (1000) for the STM32F407VET6 with 512 kbytes of flash and 192 kbytes of RAM in an LQFP100 package. **—by Colin Holland**

▷STMicroelectronics, www.st.com.

DILBERT By Scott Adams

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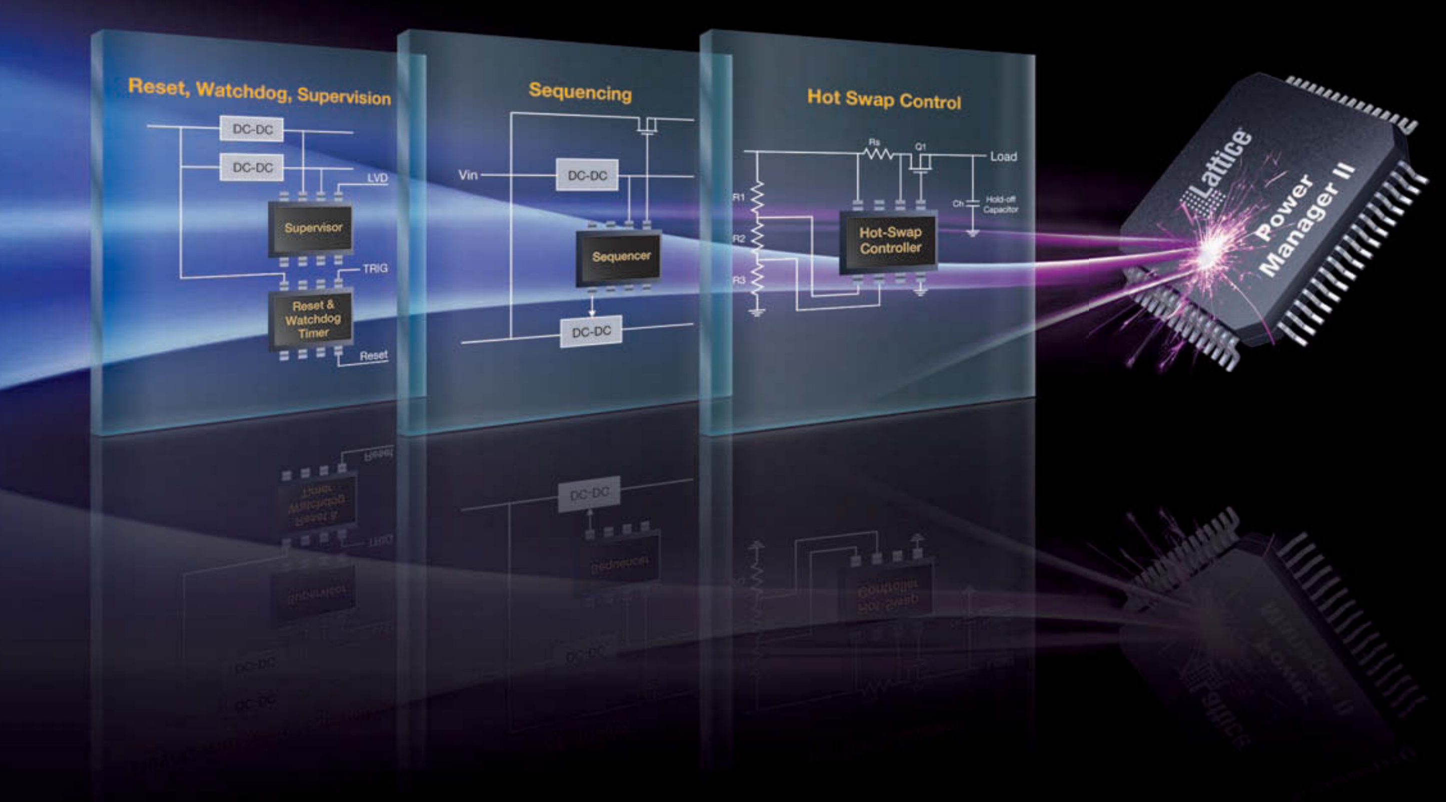

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Integer-N frequency synthesizer integrates VCO, –103-dB spurious output

Linear Technology's new LTC6946 integer-N frequency synthesizer integrates a VCO (voltage-controlled oscillator) and delivers –226-dBc (decibels referenced to the carrier)/Hz normalized, closed-loop, in-band phase noise; –274-dBc/Hz normalized, in-band flicker noise; and –103-dB spurious output. In a typical 900-MHz system, these features enable the device to achieve a closed-loop phase noise of –100 dBc/Hz at a 1-kHz offset.

The device is available in three versions: The LTC6946-1, LTC6946-2, and LTC6946-3 have frequency ranges of 2.24 to 3.74, 3.08 to 4.91, and 3.84 to 5.79 GHz, respectively. Each device has an on-chip output divider that is programmable from one through six to extend frequency coverage to as low as 373 MHz.

The device integrates a low-noise, 5.7-GHz PLL (phase-locked loop), which includes a reference divider, a phase-frequency detector with a phase-locked indicator, an ultra-low-noise charge pump, and an integer-feedback divider to achieve low-noise PLL operation. The PLL circuit tightly couples to a low-noise VCO and to internal self-calibration to ensure optimum VCO-resonant tuning. The VCO requires no external components. An on-chip SPI (serial-peripheral-interface)-compatible, bidirectional port allows frequency tuning and control and read-back of register and loop-status information.

The LTC6946 integer-N synthesizer integrates a VCO for improved performance.

The frequency synthesizer enhances the performance of multiband base stations supporting LTE (long-term-evolution), CDMA (code-division-multiple-access), WCDMA (wide-band-CDMA), UMTS (Universal Mobile Telecommunications System), GSM (global-system-for-mobile)-communications, and WiMax (worldwide-operability-for-microwave-access) standards. The device suits use in point-to-point broadband wireless-access, military, avionics, and test-and-measurement applications.

The PC-based PLLWizard design-tool software is available to facilitate interactive control and interface with the LTC6946's evaluation board. Designers can download the tool from www.linear.com/synthesizers and use it to perform simulations and optimization and then interactively verify their designs on a demonstration circuit. All versions of the LTC6946 operate at –40 to +105°C and are available in 4×5-mm, 28-lead, plastic QFN packages. Prices start at $5.75 (1000).—**by Fran Granville**

▷**Linear Technology Corp**, www.linear.com/product/LTC6946.

FPGA provides a board tester in a chip

10.20.11

Asset InterTech has expanded its ScanWorks platform for embedded-instrument engineers with tools to select instruments, set parameters, and insert them into FPGAs to function as PCB (printed-circuit-board) testers. The FCT (FPGA-controlled-test) system operates the board tester in a chip from a drag-and-drop user interface to perform validation, testing, and debugging. According to the company, escalating gate densities make FPGAs an effective platform for embedded test-and-measurement applications. Higher speeds and greater complexities have increased the electrical sensitivities of chips and boards to the point at which physical probes provide inadequate test coverage and unreliable results.

PCB-design projects can encounter delays because engineers cannot validate the hardware on the board until after completion of the firmware or operating-system-software development. FCT, in contrast, does not depend on any product software. Instead, designers can insert a board tester, bring up and wring out first prototypes of a design, and then remove the tester. If they need it later in the product's life cycle, they can insert it again, or a part of it can remain in the FPGA.

ScanWorks automates practically all of the FCT process. It selects instruments or instrument functions from a library and matches them with a description of one of the supported FPGA devices in another ScanWorks library. After a user sets the configuration parameters on the selected instruments, ScanWorks automatically generates all of the constructs for the embedded tester, facilitates the synthesis of the instrument code into the firmware the FPGA requires, and creates the software image of the tester to program the FPGA. ScanWorks then inserts the tester in the FPGA and provides a drag-and-drop user interface to operate and manage the tester. FCT's abilities expand the coverage of ScanWorks' other nonintrusive technologies, including boundary-scan test, processor-controlled test, and high-speed-I/O validation. ScanWorks FCT will become available in December 2011 from Asset InterTech and its distributors. A development license sells for $35,000.

—by Colin Holland

▶**Asset InterTech**, www.asset-intertech.com.

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Rotary Potentiometers: There Must Be a Better Option

Q: I'm trying to use a potentiometer (pot) in the feedback loop of an op amp circuit, but the adjustment is too sensitive. Do you have any suggestions on how to improve the performance of this circuit?

A: The first thing I would tell you is to be careful when using pots in feedback loops, especially at higher frequencies. Wire wound pots have lots of inductance and can cause instability. Watch out for carbon pots as they are noisy.

Here are a few things you can try, however. Depending on your situation, you can add a series resistor and use the pot to "fine tune" the value you need. Sized appropriately, the pot sensitivity will be reduced greatly. You can also put the pot in parallel with the feedback resistor. Again, sizing the feedback resistor value is critical as to what contribution the pot will play. The advantage of this option is it allows you to go all the way to zero ohms.

A better option is to use a digitally controlled potentiometer or "digiPOT," which are extremely accurate and avoid typical pot issues such as wear out, vibration, drift, size, mechanical adjustment, and environmental issues, to name a few. Several options are available for the digital control (SPI, I^{2}C, push button, and up/down interface), and the adjustment is accurate and repeatable. A digiPOT can also be used as a rheostat, which is a pot with one of the end terminals tied to the wiper to form a variable resistor. digiPOTs work in both noninverting and inverting op amp configurations.

The bandwidth of these parts covers a wide range as a function of the resistor value. For example, a digiPOT set at 1K ohms has about 5 MHz of bandwidth, whereas a resistor setting of 10K ohms has a bandwidth of 500 kHz. These parts are extremely versatile and offer the designer a new tool for their "tool box." Low power, small footprint, and solid-state reliability make digiPOTs a very attractive alternative to the "old fashioned" option.

Even though they are simple building block devices (as most components are), there is a fair amount of detailed information to be considered. The datasheets for these devices (and all Analog Devices components) contain a wealth of comprehensive information, so a thorough read is recommended to optimize your design experience.

To Learn More About digiPOTs
http://dn.hotims.com/34946-1000

Contributing Writer John Ardizzoni is a Technical Product Manager at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 30 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askjohn

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App enables consumer conveniences with wireless memory, NFC technology

STMicroelectronics recently introduced the M24LR64 wireless memory, which can transmit and receive information from an application to a smartphone containing NFC (near-field-communication) technology or to an industrial RFID (radio-frequency-identification) reader, allowing for rapid transactions, data exchange, object identification, and tracking.

NFC operates at 13.56 MHz and is finding use in smartphones to enable customers to make payments, such as for public transit and in convenience stores, using their mobile devices. The technology can also permit communication between NFC-enabled devices.

According to market researcher IHS iSuppli, partnerships between major US wireless carriers and credit-card companies will drive NFC technology into 30.5% of all handsets in 2015.

The M24LR64 wireless memory operates on the Android operating system, which connects an NFC-enabled smartphone to a prototype temperature recorder.

The dual-EE (energy-efficient) application, which operates on the Android operating system, is fully compatible with STMicroelectronics' M24LR64 wireless memory. The application connects an NFC-enabled smartphone to a prototype temperature recorder featuring the M24LR64 and demonstrates data transfer and storage. These features can work in medical devices, home appliances, consumer electronics, and meters.

The dual-interface M24LR64 EEPROM can connect directly to wireless antennas, such as those in RFID tags, to transfer data through the energy in radio waves between an RFID or an NFC reader and an electric tag attached to an object, allowing reading or updating of the equipment when it is off. It communicates with RFID and ISO15693-capable NFC readers and with the system's own processors. It also features a 32-bit-password data-protection scheme, enabling control of wireless read- and write-memory access. The device has a low-power wired-I^2C (inter-integrated-circuit) interface to a microcontroller or a chip set and sells for 72 cents (1000).

—by Fran Granville

▷**STMicroelectronics**, www.st.com.

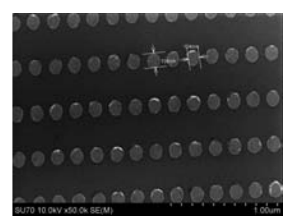
Researchers aim for energy-harvesting CPUs

The National Science Foundation and the Nanoelectronics Research Initiative of Semiconductor Research Corp recently awarded a team of researchers from VCU (Virginia Commonwealth University) two grants totaling $1.75 million to create powerful, energy-efficient computer processors that can run an embedded system without battery power. The researchers based their findings on a paper published by the VCU research team in the August issue of *Applied Physics Letters*. The technique replaces transistors with tiny nanomagnets that can also process digital information, theoretically reducing the heat dissipation by a factor of 1000 to 10,000, according to VCU.

Researchers at the VCU School of Engineering led the team, which is working with colleagues from the University of Virginia—Charlottesville, the University of Michigan—Ann Arbor, and the University of California—Riverside, to translate its theoretical work into a computing device.

"The purpose of this work is to establish a new paradigm for digital computing, which will be extremely energy-efficient and hopefully allow us to pack more and more computing devices onto a chip without having to worry about excessive heat generation," says Supriyo Bandyopadhyay, co-principal investigator for the study and a professor of electrical and computer engineering at VCU. "This [discovery] will allow us to increase the computational prowess of computers beyond what is available today."

A new technique replaces transistors with tiny nanomagnets that can also process digital information, theoretically reducing the heat dissipation by a factor of 1000 to 10,000 (courtesy Virginia Commonwealth University).



As processors have shrunk in accordance with Moore's Law, engineers are packing more and more transistors onto a chip, creating a challenge for efficiently removing the heat that the transistors generate. Reducing the amount of dissipated heat when the transistor switches is considered to be the best approach to alleviating this problem.

According to Bandyopadhyay and Jayasimha Atulasimha, an assistant professor of mechanical and nuclear engineering in the VCU School of Engineering and co-principal investigator on the project, this research could lead to a type of digital computing system for medical devices, such as processors that physicians could implant in an epileptic patient's brain that monitor brain signals to warn of impending seizures. This processor would run by harvesting energy only from the patient's head movements, without requiring a battery, they claim.

—by Dylan McGrath

▷**Virginia Commonwealth University**, www.vcu.edu.

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VOICES

Gordon Nuttall: turning layoff lemons into start-up lemonade

Armed with a bachelor's degree in electrical engineering, Gordon Nuttall went from college to work for Hewlett-Packard, where he put his engineering skills to use in areas such as digital imaging and new-business creation. Thirty-one years later, during the economic downturn of 2008, Nuttall was one of the many tech-industry employees to be laid off. Instead of taking an early retirement or seeking a position similar to the one he had just lost, Nuttall did what some might call crazy: He set out to form a start-up. Now, three years later, Nuttall and the team at Couragent Inc aren't just surviving the still-cold economy, they are growing and moving their Flip-Pal mobile scanner toward new markets. The chief executive officer recently spoke with *EDN* about the choices he made in turning a layoff into an opportunity. Excerpts of that conversation follow. Look for the full interview at www.edn.com/111020pulsea.

You had been with HP for more than 30 years. How did you react to being downsized in 2008?

A We call it "WFRed." WFR: workforce reduction. So we called ourselves the WFRers. We formed a group of people who met socially and did things together to replace that interaction you would get in the company. That social interaction tends to get lost when you leave a company.

Are these the people who helped you start Couragent?

A Some, yes. But others I had known from before and are just really talented people. That [fact] was one thing that was instrumental about the [large-scale industry] downsizing and economy: It makes for a lot of really fantastic talent out there. If I started a new company, I would never be able to recruit those people away from their old jobs. But a start-up gives people a chance to think about a new way of doing their work and what their real passion is. That's one of the ways I think the downsized economy can be turned into lemonade rather than lemons. People get a chance to do something that, in a corporate gig, they might not have ever ventured out to try. Sometimes you need to be upstaged out of your comfort zone, and then you find out that you can do so much more than you ever thought you would within the confines of a company.

Where did the name Couragent come from?

A We started the company based on our five foundational values: courage, integrity, collaboration, innovation, and care. When you take the first four letters of courage, our first value—*cour*—means heart in the old Latin derivative. And then "agent." When we talk to our team, they are "couragents," agents of heart. In that talk, we speak not only from our logic but also from our hearts, and the things that matter to us are not just facts and figures but also who we are as a people. The name reflects a lot about our company.

Any words of advice for the many talented engineers out there who have been downsized and may be wondering what to do next?

A It's very common to want to find a job like the one that you had before. Well, that's kind of slim pickings these days. I was a program manager, and big corporations aren't really hiring at that management level. I became really involved in professional-networking groups. I really encourage people to join a networking group or to become more proficient at talking with people and getting to know other areas that you normally would not have come in contact with when you were in a company. Be out there, and do a lot more networking.

I also think that the employment model of the future and the one we are using with Couragent involves multiple streams of income, where people are independent consultants and they work under a 1099 contract to one or maybe several gigs at the same time. I would suggest that people form LLCs [limited-liability companies] to take advantage of tax benefits. And go to the conventions; join the associations that are the industry-leading professional organizations. It looks good on a résumé, and it keeps you speaking the general lingo of the industry.

You left college, went into this corporate world at HP, were downsized, and are now here in this whole new life. Are you happy?

A I'm pursuing my passion. I sometimes will give presentations to groups, and I will say that I'm unemployable now. For me to go back to a corporate gig—where you have to do all the politics, and decisions take forever, and you have to get three doubles of an approval—I could never go back to that. With this small company, when we need to make a decision, we just put our heads together and go for it. Once you've experienced that passion for action, you might never want to go back. Some days I wonder what the heck I am doing starting a company at 56 years old. Maybe there is a fine line between crazy and totally gassed.

Everybody thinks it's the younger folks who are doing all the entrepreneurial, innovation stuff. But we're doing a great job, enjoying ourselves, and have a very solid business plan ... . So this has got a lot of nice aspects to it.**—interview conducted and edited by Suzanne Deffree**

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BY BONNIE BAKER

Designing with temperature sensors, part two: thermistors

Thermistors, which range in price from 10 cents to approximately $25, find use in applications from automotive monitoring and exhaust-emissions control to ice detection, skin sensors, blood and urine analyzers, home appliances, mobile phones, base-station laser drives, and battery-pack charging. Thermistors are either NTC (negative temperature coefficient) or PTC (positive temperature coefficient). NTC thermistors best suit precision temperature measurement, and PTC devices best suit switching applications. This column focuses on NTC devices.

The most prevalent NTC-thermistor configuration uses the resistance-versus-temperature characteristics of the device. The thermistor must operate in a "zero-power" condition, which implies that current or voltage excitation to the thermistor does not induce self-heating. **Figure 1** shows the temperature response of a 10-kΩ NTC thermistor. Note the nonlinearity.

Typically, the 25°C rating for thermistors is 1 kΩ to 10 MΩ. Because thermistors are resistive elements, they require current excitation from a voltage or a current reference. Although thermistors have better linearity than that of thermocouples, they still require linearization in most temperature-sensing circuits.

An empirical third-order polynomial, using the Steinhart-Hart thermistor equation (**Reference 1**), or a look-up table can correct the nonlinear response of the thermistor in software. The Steinhart-Hart equation provides approximately ±0.1°C accuracy over the full temperature range of the thermistor. In the **equation**, $\ln R_T = B_0 + B_1/T + B_3/T^3$, T is the temperature of the thermistor in kelvins; B_0, B_1, and B_3 are constants that the thermistor manufacturer provides; and R_T is the thermocouple resistance at T.

If you use these techniques to determine temperature, the nonlinearity of the thermistor still produces a nonlinear voltage output with a current-source excitation. The differential resistance for a 10°C change at high temperature is significantly smaller than the resistance at low temperatures. You can address this issue by using a high-resolution ADC, but you will lose some bits. An alternative is to implement linearization with the analog hardware.

A simple approach to a first-level analog linearization of the thermistor output is to use the circuit in **Figure 2**. The thermistor is in series with a standard, 1%-tolerant, metal-film resistor, and the temperature response and linearity of the system show that it responds to temperature in a linear manner over a limited temperature range. The linearization resistor's value, R_{USER}, should equal the magnitude of the thermistor at the midpoint of the temperature range of interest, creating a response in which the resistive network is at its steepest at this midpoint. If your design requires high precision, this range is typically ±25°C at approximately the midpoint temperature.

The circuit in **Figure 2** uses an ADS7822 from Texas Instruments to sense the voltage output (V_{OUT}) of the series configuration of the thermistor (R_{NTC}) and the series resistor. If the ADS7822 has low acquisition speed, the input circuitry to the converter will settle before conversion.

Read part one of this series, on sensor types, at http://bit.ly/rpSnOp. EDN

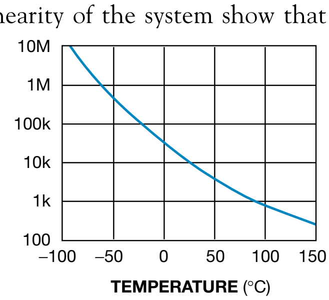

Figure 1 The temperature response of a 10-kΩ NTC thermistor is nonlinear.

REFERENCE

1 Steinhart, JS, and Stan R Hart, *Deep Sea Research*, Volume 15, Elsevier, 1968.

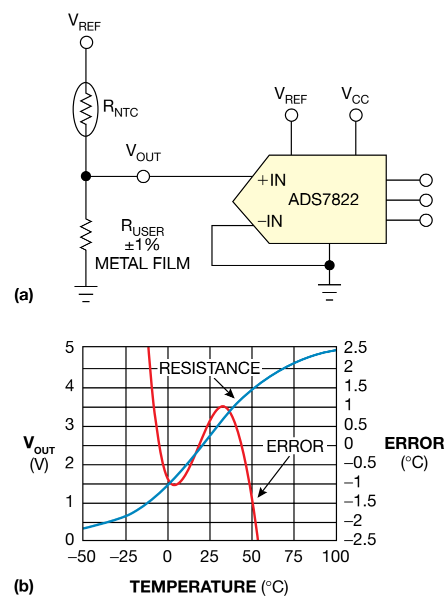

Figure 2 This circuit provides a simple approach to a first-level analog linearization of the thermistor output (a). In series with a standard, 1%-tolerant, metal-film resistor, the thermistor has a temperature response and linearity showing that it responds to temperature in a linear manner over a limited temperature range (b).

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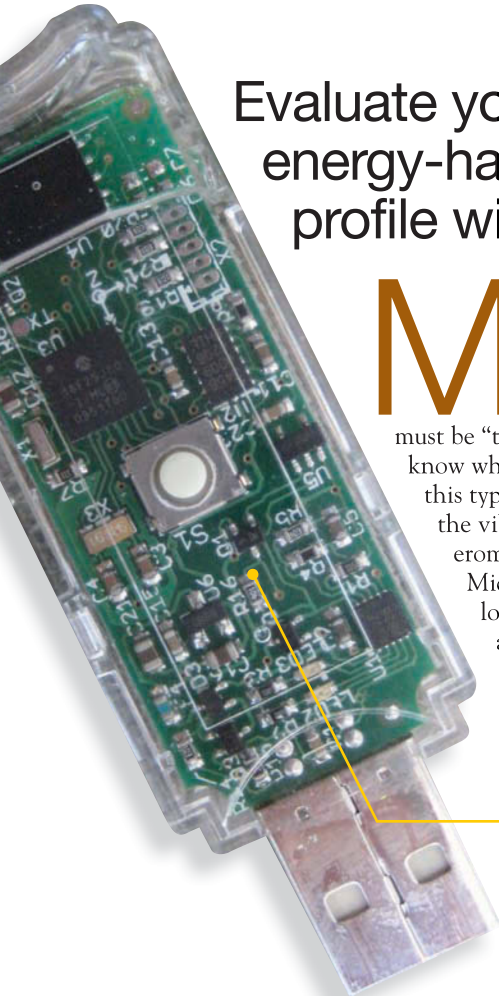
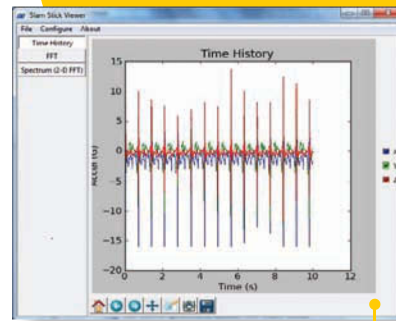
Evaluate your application's energy-harvesting vibrational profile with a Slam Stick

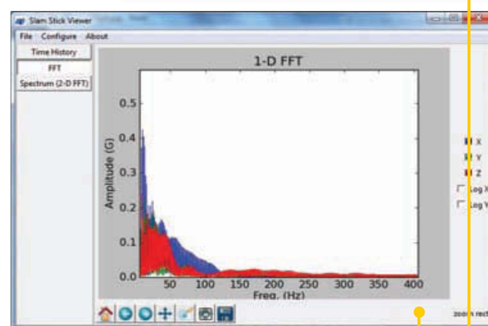


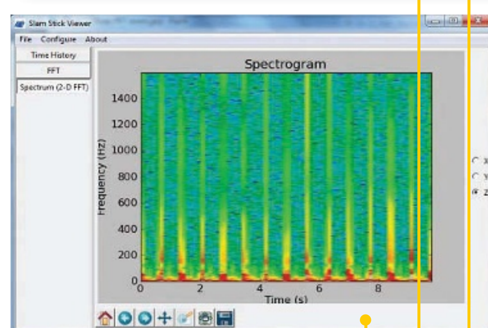
Midé Technology's energy-harvesting devices rely on resonant harvesting. To extract the maximum available vibrational energy from their environment, the harvesters must be "tuned" to match the vibration. To know whether your application is suitable for this type of harvesting, you must determine the vibrational profile by using an accelerometer. To ease the task of profiling, Midé designed the Slam Stick—a data logger that measures acceleration in all three axes—with the form factor of the familiar USB (Universal Serial Bus) stick.

The Slam Stick uses an 8-bit Microchip PIC18F25J50 microcontroller, which integrates a full-speed USB 2.0 transceiver and a 10-bit, 10-channel ADC. The Slam Stick also uses Analog Devices' three-axis ADXL345 accelerometer. According to Tim Gipson, a design engineer at Midé, using a high-Q resonating piezoelectronic beam to harvest energy requires accurate knowledge of the vibration frequency, ideally within 1 to 2 Hz. The ADXL345 internally generates its own sampling clock; however, this clock frequency can vary from part to part. In response, Midé runs an accurate, 32-kHz oscillator along with the accelerometer to determine its actual sampling rate and stores a correction factor in the recording file, giving fractional-hertz accuracy.

The reverse side of the Slam Stick shows its lithium-polymer battery. The device charges in one to two hours after you plug it into a USB port. A green LED indicates when it's ready to go. The company evaluated some thin-form-factor supercapacitors early in the design, but the lower self-discharge and flatter discharge curve of the lithium-polymer battery keep the design small and simple.







The Slam Stick works with its open-source analysis software. The screen on the top shows the recorded g force versus time over the Stick's default 10-sec recording period. The middle screen shows an expanded view of an FFT (fast Fourier transform), which converts the amplitude versus time of the data to frequency versus time. The bottom screen shows a spectrogram of the shoe strike.

The software doesn't currently tell you how much energy is being generated because the amount of energy available for harvesting depends on several factors beyond the frequency and amplitude. For example, the same piezoelectric beam with a small proof mass at the end versus a large proof mass in the center might tune to the same frequency but have different power outputs in the same environment.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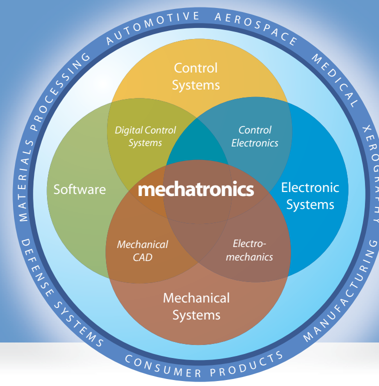
MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



No fighting

In life and in mechanical design, keep the peace.

Most engineers have taken a course on the design of machines and machine elements. These courses, however, often overlook the insight that expert machine designers have gleaned from years of practice. Guiding principles—for example, keep complexity intrinsic, keep functions independent, improve designs with self-help, and plan load paths in assemblies—are not well-publicized. One of the most important guiding principles is exact-constraint design, and **references 1** and **2** provide material on that topic, with **Reference 2** serving as the source for much of this column.

Precision machines are essential elements of an industrial society. A precision machine is an integrated system that relies on the attributes of one component to augment the weaknesses of another component. Characteristic to all precision systems is the high level of determinacy they require. Predictable and reproducible behavior is a key quality that only carefully designed, robust mechanics and control systems can achieve. To achieve excellent and predictable behavior, the mechanisms require, among other things, exact constraint—just enough constraint to define a position or motion. Unlike overconstrained designs, exactly constrained designs boast a repeatable position, easy assembly, and robustness to wear and environment. They have no binding, no play, no internal stress, and no loose-tolerance parts.

A 3-D object has six degrees of freedom—the number of independent coordinates necessary to describe a system's motion—three translations and three rotations. Selectively constrain these degrees of freedom to obtain the desired motion or structure. If you rigidly constrain a component at more places than necessary—by, for example, placing three bearings on one shaft—these places will "fight" with each other.

Kevin C Craig, PhD, is the Robert C Greenheck chairman in engineering design and a professor of mechanical engineering at Marquette University's College of Engineering. For more mechatronic news, visit mechatronicszone.com.

The design of high-quality precision machines depends primarily on an engineer's ability to predict how the machine will perform before he builds it. The most important factors affecting the quality of a machine are its accuracy; its precision, or repeatability; and the resolution of its components and the manner in which they are combined. Accuracy is the ability to tell the truth, precision is the ability to tell the same story over and over again, and resolution is how much detail the story has. Designing a machine that has good accuracy, precision, and resolution is not a black art.

Consider the use of linear drives for scanning. They often comprise a motor attached to a lead screw, which in turn drives the scanning carriage. A first design shows a cyclic error in linear motion (**Figure 1a**). Trying more accurate machining, better part alignment, and a more expensive lead screw yields no success. A constraint analysis shows that the design is overconstrained. The motor attaches rigidly to the lead screw, so the motor requires only one constraint: to prevent the rotation of its housing. The compound flexure eliminates the problem by eliminating the need for an expensive lead screw, accurate machining, and assembly steps (**Figure 1b**).

Understanding how to transform basic physical principles into working concepts with predictable behavior is the key to achieving high accuracy, high speed, and high reliability. EDN

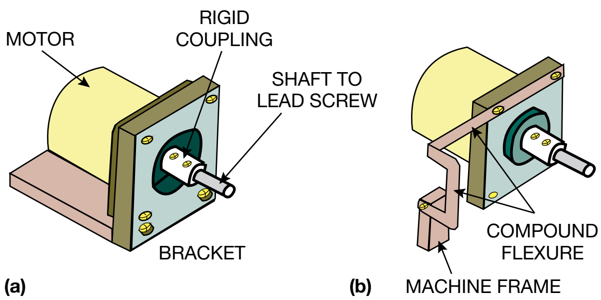


Figure 1 A first design shows a cyclic error in linear motion (a). A constraint analysis shows that the design is overconstrained. The compound flexure eliminates the problem by eliminating the need for an expensive lead screw, accurate machining, and assembly steps (b).

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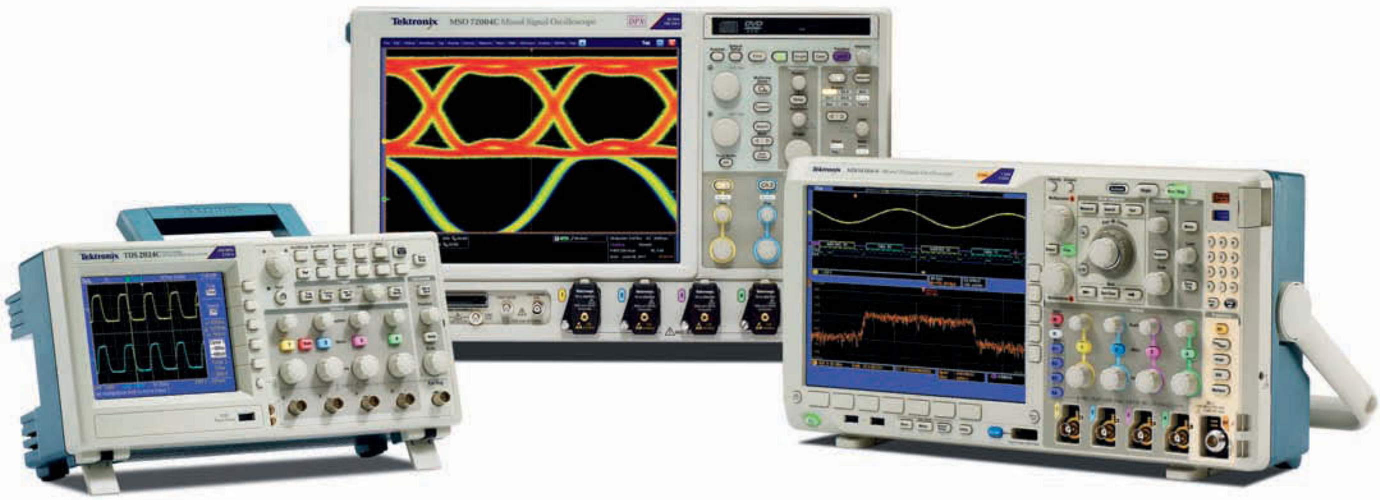
BY HOWELL MITCHELL • SILICON LABORATORIES

When measuring ultra-low-jitter devices and equipment, engineers must constantly ask whether the measurement values are from the DUT (device under test) or from the test equipment. Engineers are also always looking for methods of expanding the reach of the equipment at hand. This article describes some practical ways to handle situations in which clock signals have been divided down from higher-frequency VCOs (voltage-controlled oscillators).

IMAGE: THINKSTOCK

Oscilloscopes Don't Change the World.
Engineers Do.



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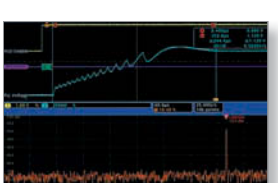

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Most modern equipment that measures jitter can be placed into one of two broad categories: time domain or frequency domain. Time-domain equipment typically comes in the form of a high-speed digital oscilloscope with high single-shot sampling bandwidth. Frequency-domain equipment usually comes in the form of a spectrum analyzer, a spectrum analyzer with phase-noise measurement capability, or a phase-noise analyzer. Each of these two categories of equipment has its own set of advantages and disadvantages. However, both measure the same phenomena, albeit with different approaches.

Peak cycle-to-cycle jitter is the maximum difference between consecutive, adjacent clock periods over a fixed number of cycles—typically, 1000 or 10,000. It is used whenever there is a need to limit the size of a sudden jump in frequency. For example, when driving a PLL (phase-locked loop), you may want to limit the size of an instantaneous change in frequency to ensure that downstream PLLs remain in lock (**Reference 1** and **Figure 1**).

The peak-to-peak period jitter is the difference between the largest clock period and the smallest clock period for all clock periods within an observation window—again, typically 1000 or 10,000 cycles (**Figure 2**). It is a useful specification for guaranteeing the setup-and-hold time of flip-flops in digital systems. "Peak-to-peak" refers to the difference between the smallest and the largest sampled period value during a measurement.

TIE (time-interval-error) jitter, or accumulated jitter—also known as phase jitter—is the actual deviation from the ideal clock period over all clock periods (**Figure 3**). It includes jitter at all jitter-modulation frequencies and commonly finds use in WAN (wide-area-network) timing applications, such as SONET (synchronous optical network), synchronous Ethernet, and OTN (optical-transport networking).

AT A GLANCE

- Time-domain equipment is better than frequency-domain systems at measuring data-dependent jitter, making it useful for high-speed serial links that use SERDES (serializer/deserializer) technology.
- High-quality frequency-domain instruments have lower noise floors than their time-domain counterparts, making frequency-domain units the instruments of choice for ultra-low-phase-noise clock-signal measurements that are free of data-dependent jitter.
- An instrument's noise floor can become the limiting factor of a measurement of phase noise of very-low-jitter clocks at low clock frequencies.

You can create various types of statistics, such as rms (root-mean-square), peak-to-peak, cycle-to-cycle, period, and TIE jitter, although some are more commonly used than others. Whenever peak-to-peak statistics are used, the number of samples taken must be large enough to produce confidence in the measurement. Such measurements typically include 1000 to 10,000 samples.

Time-domain equipment can directly measure peak-to-peak, cycle-to-cycle, period, and TIE jitter. This measurement approach permits the measurement of jitter for low-frequency clock, or carrier, signals. By employing FFTs (fast Fourier transforms), digital filters, and other techniques to postprocess the data, you can integrate the phase-noise value over a band of frequencies to generate rms-phase-jitter values. Time-domain equipment is better than frequency-domain systems at measuring data-dependent jitter, making it useful for high-speed serial links that use SERDES (serializer/deserializer) technology.

Frequency-domain equipment cannot directly measure peak-to-peak, cycle-to-cycle, or period jitter; its native ability is to measure the rms power of a signal in a given frequency band. Frequency-domain equipment is also awkward for measuring data-dependent jitter. However, high-quality frequency-domain instruments have lower noise floors than their time-domain coun-

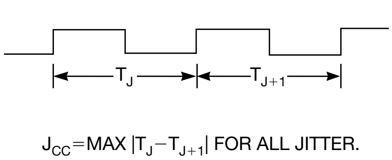


Figure 1 When driving a PLL (phase-locked loop), you may want to limit the size of an instantaneous change in frequency to ensure that downstream PLLs remain in lock.

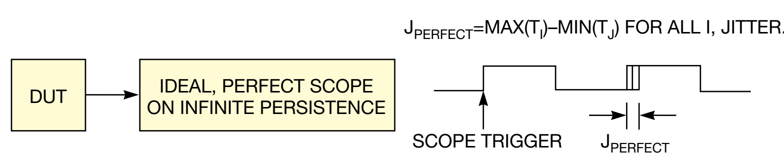


Figure 2 The peak-to-peak period jitter is the difference between the largest clock period and the smallest clock period for all clock periods within an observation window—typically 1000 or 10,000 cycles.

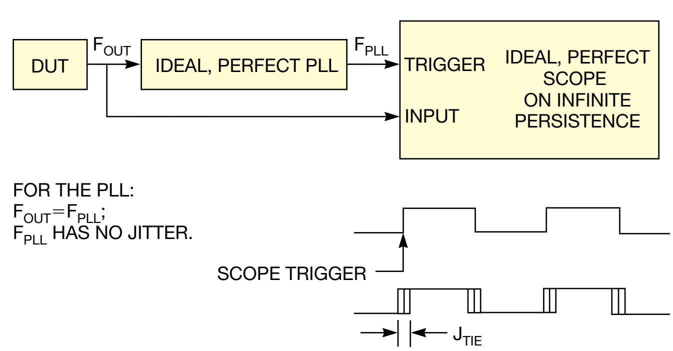


Figure 3 TIE jitter is the actual deviation from the ideal clock period over all clock periods.

terparts, making frequency-domain units the instruments of choice for ultra-low-phase-noise clock-signal measurements that are free of data-dependent jitter (**Table 1**).

Because this article focuses on the measurement of low-jitter clock signals, it omits further discussion of time-domain equipment except to mention that you can use various mathematical-estimation and -translation approaches to go from one type of jitter measurement to another. For example, it is possible to use a crest factor and a desired BER (bit-error rate) to go back and forth between peak-to-peak and rms jitter. Another example is using an FFT of time-domain data to provide frequency-domain information and filtering. However, most of these techniques rely on mathematical models, which may be good approximations in most situations but have limitations. As such, you should use them only carefully.

One issue that bears further investigation is the effect of clock, or carrier, frequency on the jitter measurement. It is intuitive that a clock signal divided down by an ideal divider will have the same clock edge jitter at both its input and output (**Figure 4**). In the **figure**, the top jittered signal with frequency F_O is divided by two using a perfect divider to produce a clock frequency of $F_O/2$. Both clock signals have the same jitter, J_O. Note that the jitter energy of the lower clock signal is half that of the higher clock signal because there are half as many edges in a given interval of time.

The intuition that J_O is the same for the two clock signals is for the most part true, despite the fact that the phase noise of a clock signal that is divided by two will be 6 dB lower than the phase noise of the original clock signal. Note that, for division by two, 6 dB=20×log2 (**Reference 2**).

The following example illustrates the effect of division by powers of two for both phase noise and jitter. These measurements employ a Silicon Laboratories Si5324 PLL device (**Figure 5**). Note that the high-speed VCO resynchronizes the output clock, regardless of the final output frequency, meaning that the edge shape and placement should be the

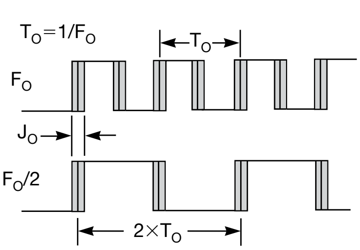
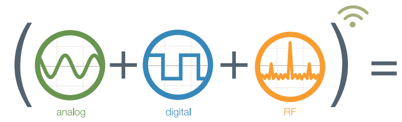


Figure 4 It is intuitive that an ideal divider divides down a clock signal that has the same clock-edge jitter after the divider as it has before the divider.

TABLE 1 DIFFERENCES IN TIME- VERSUS FREQUENCY-DOMAIN INSTRUMENTS

	Time domain	Frequency domain
Native measurements	Peak-to-peak, cycle-to-cycle, and period jitter	Phase noise, rms phase jitter, jitter-frequency information
Advantages	Good with low-frequency clocks and data-dependent jitter	Lower noise floor, easy detection of spurs versus random jitter



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same for all possible divider values. The only difference should be that fewer clock edges occur during a given time interval. Although some retiming noise remains, the noise is the same for all of the divisor values (**Figure 6**).

The six curves in the **figure** are essentially the same but with a vertical separation of 6 dBc/Hz. The 6-dB separation is relatively constant over all offset frequencies and divisor values, with one or two exceptions. On the right side of the plot, in which the offset from the clock, or carrier, is at its largest, the relative vertical offsets between the curves are compressed. The compression increases as the clock frequency decreases. This compression becomes more pronounced as the clock frequency and the phase-noise-curve values decrease. The compression occurs because the noise floor of the Agilent Technologies model E5052B signal-source analyzer nears the value of the phase noise, or jitter generation, of the Si5324 IC. The noise floor is an issue only because of the combined effect of the ultra-low jitter of the Si5324 and the low carrier frequency. **Table 2** lists the corresponding jitter values for each of the six plots with the jitter integrated from 100 Hz to 20 MHz and all jitter values in femtoseconds rms.

Notice that the jitter increases slightly as the output frequency decreases—evidence that the output jitter is relatively constant despite the fact that 6 dB separates the phase-noise curves from one another. The rate at which the jitter increases becomes more pronounced at the lowest output frequencies. Let's examine the two sources of the increased rms-phase-noise values: instrument noise floor and aliasing.

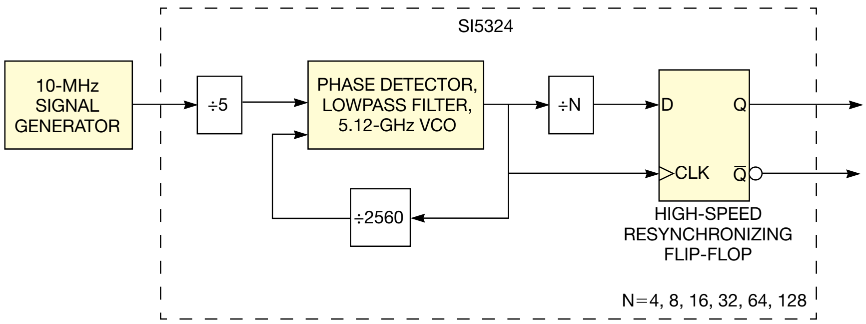

Figure 5 The measurements employ a Silicon Laboratories Si5324 PLL device.

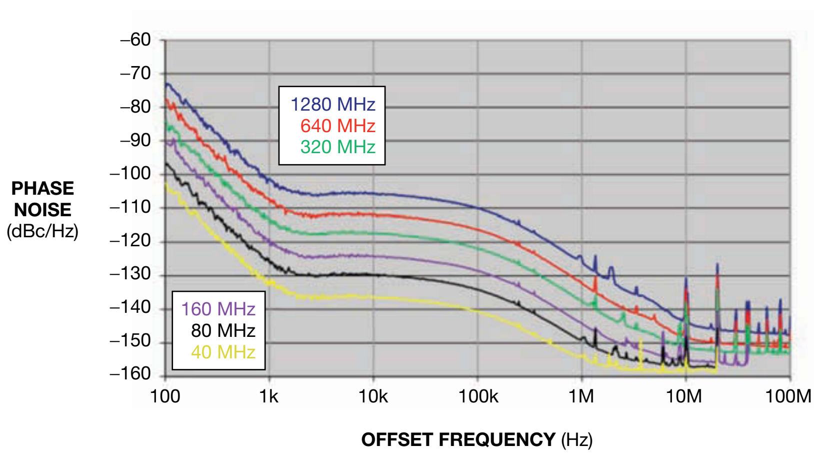

Figure 6 The high-speed VCO resynchronizes the output clock, regardless of the final output frequency, meaning that the edge shape and placement should be the same for all possible divisor values. The only difference should be that fewer clock edges occur during a given time interval.

TABLE 2 RMS-JITTER VALUES FOR DIFFERENT VALUES OF DIVISION

Color	Divisor	Output frequency (MHz)	Jitter (fsec rms)
Blue	Four	1280	441
Red	Eight	640	447
Green	16	320	461
Purple	32	160	463
Black	64	80	477
Yellow	128	40	523

NOISE FLOOR, PHASE NOISE

The instrument's noise floor can become the limiting factor of a measurement of phase noise of very-low-jitter clocks at low clock frequencies. At some point, you are measuring your equipment, not the DUT. Even though the phase-noise curves become monotonically smaller as the clock frequency decreases, the rms edge jitter remains almost constant because the phase-noise integration uses the clock period to scale the rms-jitter values.

To illustrate how this scenario occurs, consider the process of phase-noise integration to produce an rms-jitter value. Most modern phase-noise equipment produces a file that has two columns—typically, a CSV (comma-separated-value) file. One of the two columns lists the frequency offset from the clock, or carrier, frequency in hertz. The other column lists the phase-noise values at that offset frequency in decibels referenced to the carrier per hertz. Thus, the columns contain data-point pairs that describe the phase noise at a given offset from the clock frequency. Integration involves summing the area under the curve for all of the frequency-offset points after converting the decibels-referenced-to-the-carrier-per-hertz values to linear values using the following **equation**: Linear values=$10^{(\mathrm{dBc/Hz})/10}$.

The equation for the area of a trapezoid in **Figure 7** is used to find the area described by two adjacent data-point pairs. You find the area under the curve by summing the area of all of the trapezoids. The final rms-jitter value is determined by scaling the result by two factors: The value $\sqrt{2}$ comes from the fact that the data was taken as one sideband; however, the rms jitter is assumed to be dual sideband. It is usually safe to assume that the two sidebands of the phase noise are symmetric about the clock frequency. In this case, it is even safer because a limiting amp suppresses AM (amplitude modulation) and passes FM (frequency modulation) to ensure symmetric sidebands (**Figure 8**).

The other scaling factor converts the area sum so that it is no longer in UIs (unit intervals) but in units of time. This factor keeps the rms edge jitter's values relatively constant, whereas the phase-noise values change. The equation for rms jitter is expressed as follows:

$$\text{rms jitter}=\frac{\sqrt{2}}{2\pi F_C}\sum_i \frac{(F_{i+1}-F_i)\times\left(10^{\frac{(N_i+1)}{10}}+10^{\frac{(N_i)}{10}}\right)}{2},$$

where F_C is the clock frequency, N_i is the phase noise in decibels referenced to the carrier per hertz for the ith entry, and F_i is the offset frequency for the ith entry.

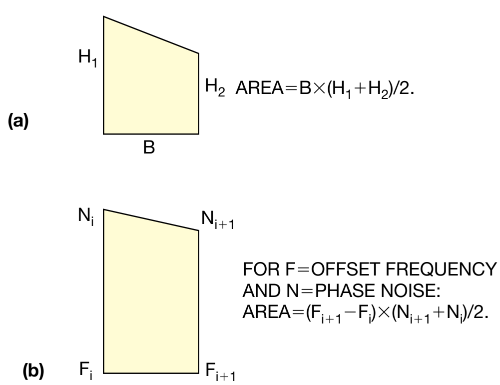

Figure 7 You find the area under the curve by summing the area of all of the trapezoids. You determine the final rms-jitter value by scaling the result by two factors.

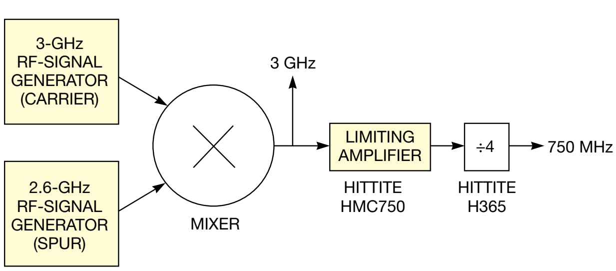

Figure 8 A limiting amp suppresses AM and passes FM to ensure symmetric sidebands.

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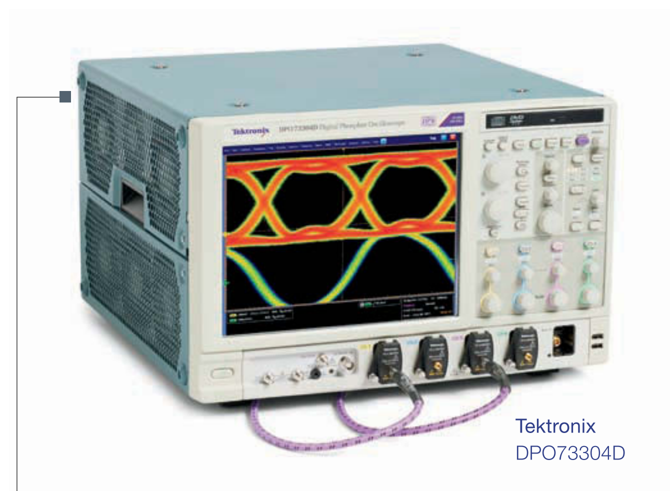

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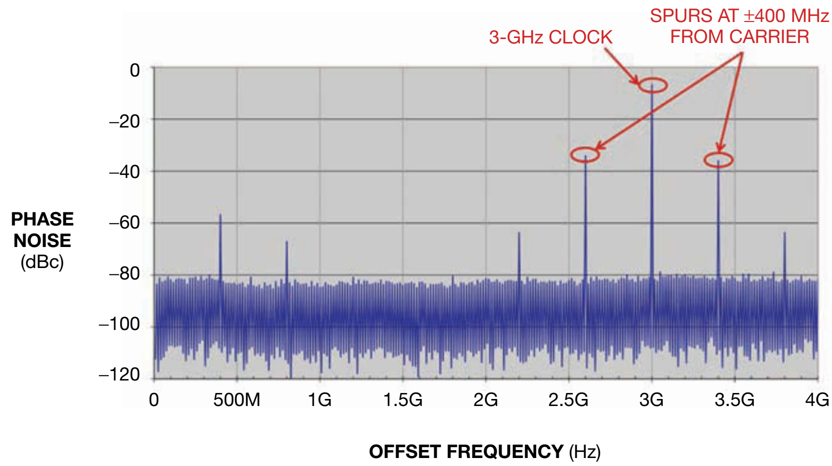

Figure 9 Symmetrical spurs occur at frequencies of 400 MHz above and below the 3-GHz clock frequency.

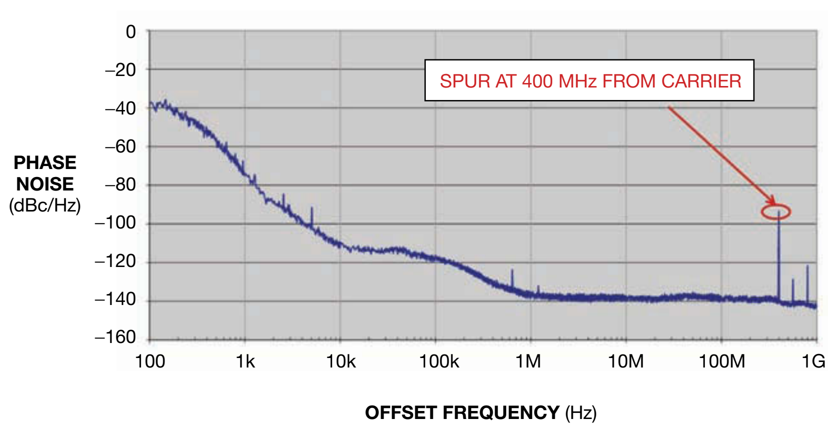

Figure 10 When the spectrum shows two equal sidebands, the phase-noise plot of the same signal combines their effect into one spur 400 MHz from the 3-GHz carrier. A divide-by-four circuit then divides down the 3-GHz signal to produce 750 MHz.

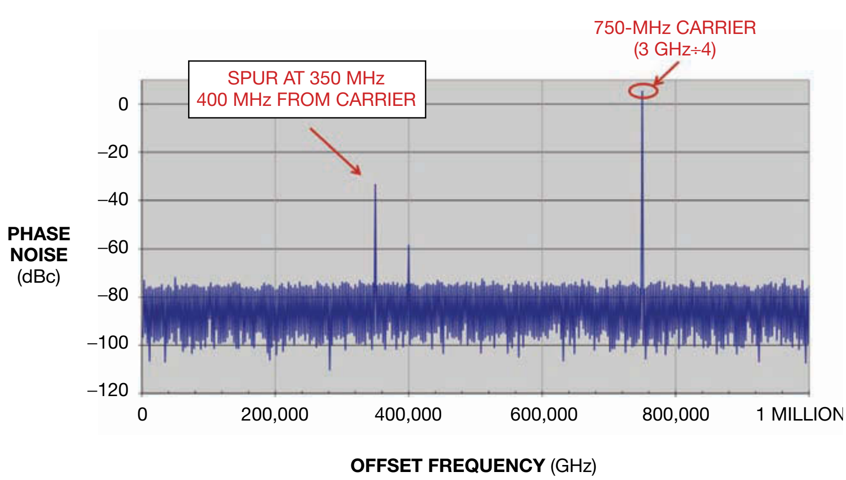

Figure 11 The spurs at 2.6 and 3.4 GHz alias down to a sideband spur at 350 MHz.

ALIASING

Aliasing is another cause of increasing rms-jitter values with decreasing clock frequency. For every division of two, the upper half of a phase-noise plot aliases down into the new lower-clock-frequency phase plot. Because phase noise is usually higher close to the clock or carrier frequency and drops off as the offset from the clock frequency increases, relatively little phase noise aliases down. However, when dividing by large numbers, the effect becomes cumulative and significant. For example, the difference between the 1280- and the 640-MHz curves in **Figure 1** is a constant 6 dB across the entire plot. As a result, you would expect that the increased rms-jitter values for the two curves in **Table 2** are due entirely to aliasing and not to the instrument's noise floor.

The spectra and phase-noise plots in **Figures 9** through **13** illustrate aliasing. The signals in these examples use AM to illustrate aliasing and are not what would be expected in a typical application. **Figures 9** and **10** show the spectra and phase-noise plots for the 3-GHz signal. The plots show symmetrical spurs at frequencies of 400 MHz above and below the 3-GHz clock frequency. When the spectrum shows two equal sidebands, the phase-noise plot of the same signal combines their effect into one spur 400 MHz from the 3-GHz carrier. A divide-by-four circuit then divides down the 3-GHz signal to produce 750 MHz.

Figures 11 and **12** show the spectra and phase-noise plots of the 750-MHz signal from the divide-by-four circuit. As a result of the division by four, the spurs at 2.6 and 3.4 GHz alias down to a sideband spur at 350 MHz. Note that 350 MHz is a frequency value that is the same 400 MHz from the 750-MHz carrier as 2.6 GHz is from the 3-GHz carrier. To further illustrate the aliasing, the 750-MHz signal is again divided down to 375 MHz. The 25-MHz spur in **Figure 13** is an alias of the spur at 350 MHz in **Figure 11**; that is, 25 MHz=375 MHz–350 MHz.

As you can see, the instrumentation's noise floor can become a limiting factor when measuring low-jitter clocks with low-frequency values. When a higher-frequency clock divides down the clock being measured, you can lower the value of the divider so that the measurement takes place at a higher frequency.

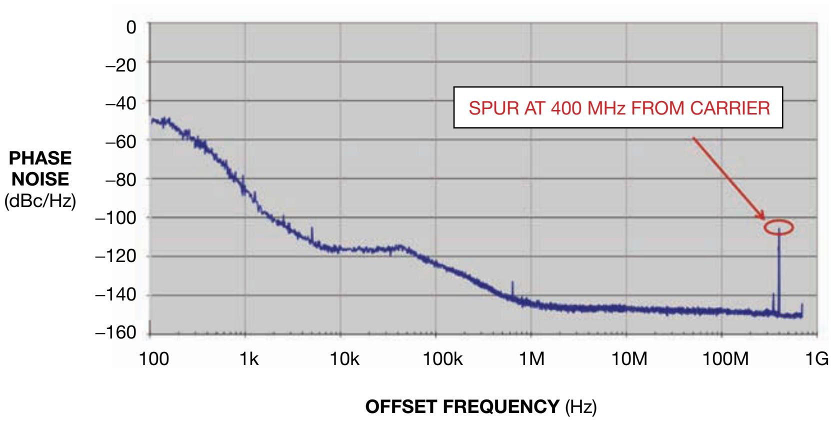

Figure 12 The 350-MHz frequency value is the same 400 MHz from the 750-MHz carrier as 2.6 GHz is from the 3-GHz carrier.

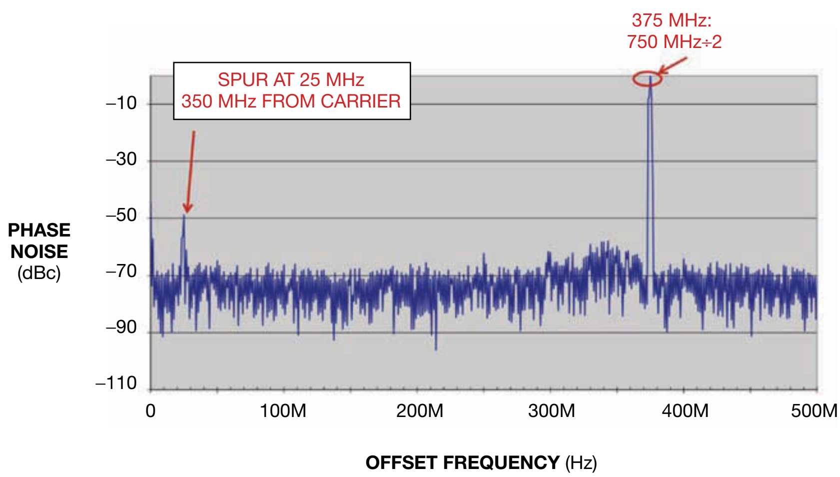

Figure 13 The 25-MHz spur is an alias of the spur at 350 MHz in Figure 11.

However, this commonly used technique removes the jitter contribution from higher-frequency jitter components that would have been aliased down by the division. Although the resulting rms-jitter values may be artificially lower, this approach is acceptable in applications in which the phase noise that is far off of the corner is relatively small. When measuring low-frequency clocks with appropriately high amounts of jitter, use time-domain equipment because the measurement can be made at the actual desired output frequency, no matter how low the clock frequency may be.EDN

ACKNOWLEDGMENT

This article originally appeared on EDN's sister site, Test & Measurement Designline, *http://bit.ly/pCHBRD.*

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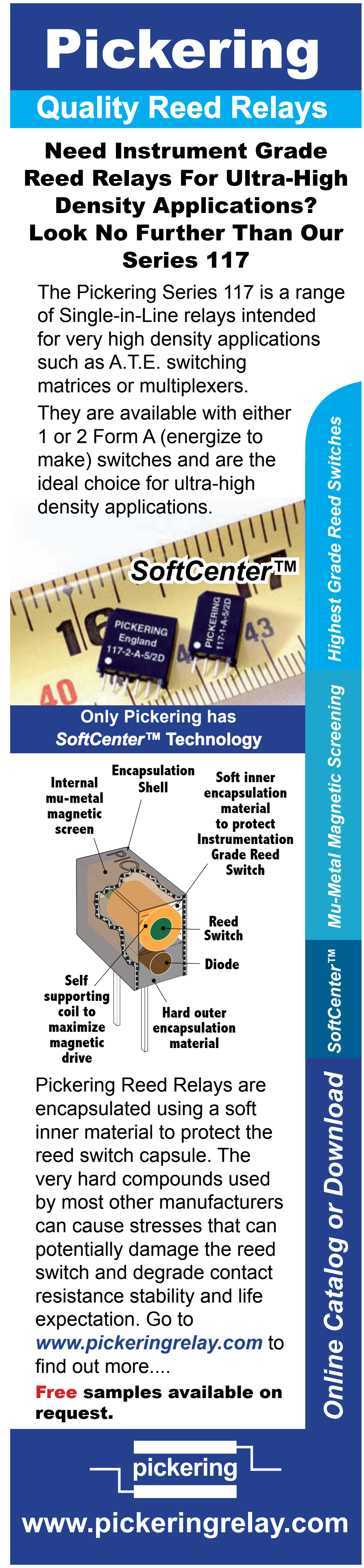
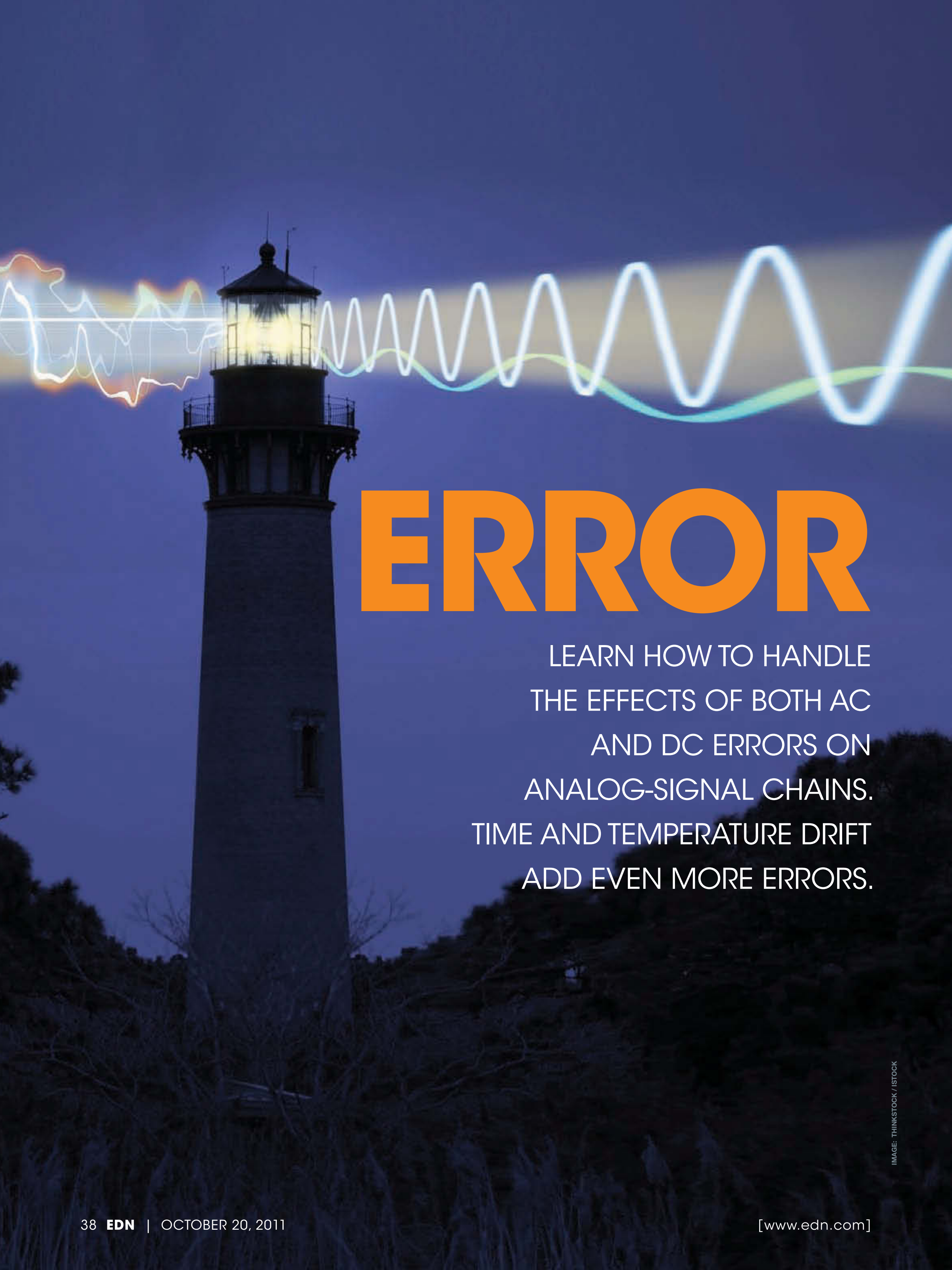
Howell Mitchell is a staff applications engineer at Silicon Laboratories, where he is responsible for product support for a family of jitter-attenuating PLL-based timing devices. Before joining Silicon Labs, he was a principal engineer at MagiQ Technologies, where he worked in quantum-key distribution. Mitchell holds five patents in phase modulation and quantum-key distribution. He received a bachelor's degree in physics from Bucknell University (Lewisburg, PA) and a master's degree in engineering from Northeastern University (Boston).





ERROR

LEARN HOW TO HANDLE THE EFFECTS OF BOTH AC AND DC ERRORS ON ANALOG-SIGNAL CHAINS. TIME AND TEMPERATURE DRIFT ADD EVEN MORE ERRORS.

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BUDGETS KEEP YOUR ANALOG-SIGNAL PATH HONEST

BY PAUL RAKO • TECHNICAL EDITOR

To deal with errors in your design's analog-signal chain, you must understand their sources in attenuators, amplifiers, multiplexers, references, and ADCs. Although Monte Carlo Spice simulations can help you handle component tolerances, keep in mind that resistor tolerances can create dc errors and that capacitors and inductor tolerances can create ac errors. The stray capacitance and inductance on PCBs (printed-circuit boards) also create ac errors. Once you establish the dc and ac errors due to component tolerances, you can examine the dc and ac errors that the ICs in the signal path cause. You can then calculate and track all of the errors with a spreadsheet to ensure that your system will meet the required specifications (**tables 1** and **2**).

Some programmers' claims that you can calibrate out all errors in software may lull you into a false sense of security regarding the errors in your design. However, dc analysis ensures that your ADC receives the required signal at its full dynamic range without clipping. A 10-bit converter has 1024 steps in its output code, so you might think it would be ideal for a 0.1%-accurate system because it has a range better than 1000-to-1. However, dc errors in the signal chain can put 100 counts of offset into the signal at the ADC, so you cannot achieve 0.1% accuracy no matter how much software correction you do. If the 100-count offset is positive, the ADC provides digital outputs only from 100 to 1024—not the full range of more than 1000 counts—so this system cannot achieve 0.1% accuracy. This situation is true even if software reduces the gain so that the ADC input does not saturate at its most positive level. Software can reduce the gain of the signal by 100 counts to compensate for the positive offset, but the signal still does not have a dynamic range of the full 10 bits.

AT A GLANCE

- Every component in the signal chain contributes ac errors, dc errors, or both.
- You must examine, analyze, and tabulate the errors in the signal chain so that the trade-offs you make ultimately yield a feasible design.
- Tiny signals and fast signals need special attention.
- You can use a spreadsheet to calculate errors.

Every component in the signal chain contributes ac errors, dc errors, or both (**Figure 1**). Other errors are due to drift, which most commonly refers to specification changes over temperature. Time drift, which contributes ac errors, refers to the changes in spec as a component ages, but the drift is so slow that engineers don't consider the errors to be normal ac errors. Electrical noise, which is inherent in the atomic vibrations due to temperature and can be a function of the quantum mechanics in a semiconductor device, also causes errors. As with so many other gray areas in analog design, you might think of time drift as low-frequency noise.

Errors, drift, and noise all conspire to make your analog-signal chain less accurate than you might hope. For this reason, experienced analog engineers would not start with a 10-bit ADC to make a 0.1%-accurate system; they would instead start with a 12- or even a 14-bit converter to leave margin for all of the analog components that contribute to the total system error. Some application engineers who work for ADC groups maintain that the analog components feeding the converter should be transparent, so that they have no effect on the converter. This scenario is at best optimistic and at worst

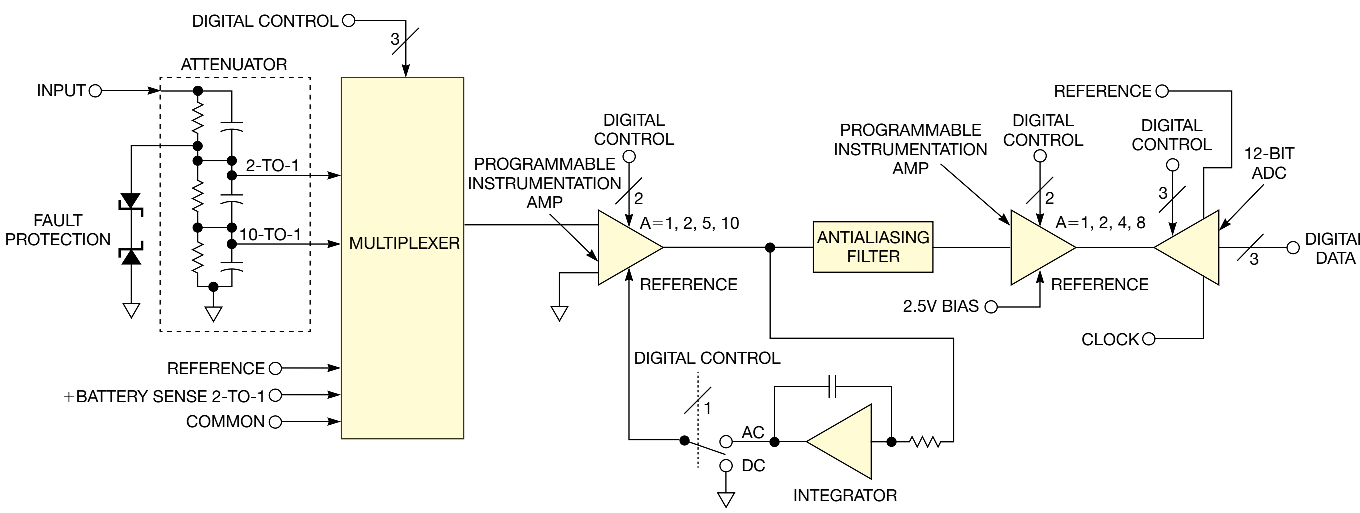
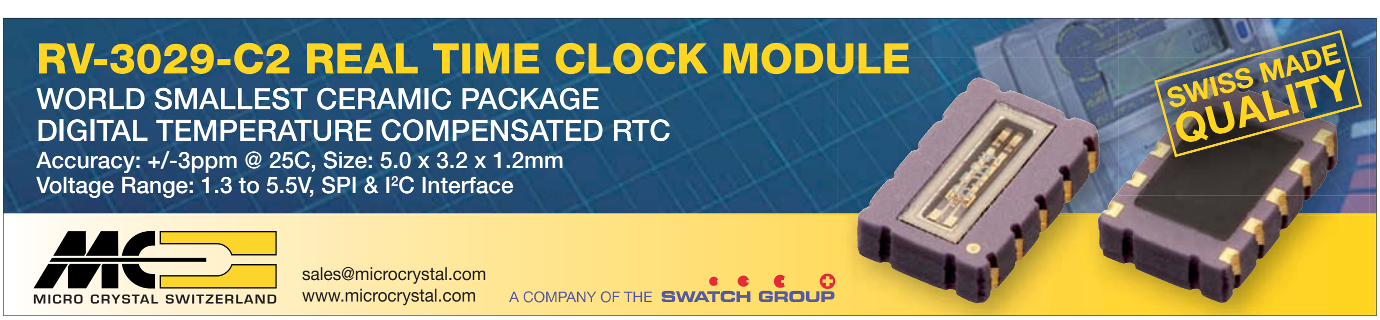


Figure 1 All of the parts in an analog-measurement signal path are subject to ac, dc, drift, and noise errors. Power-supply noise can also creep into the signal chain and ruin your measurements.



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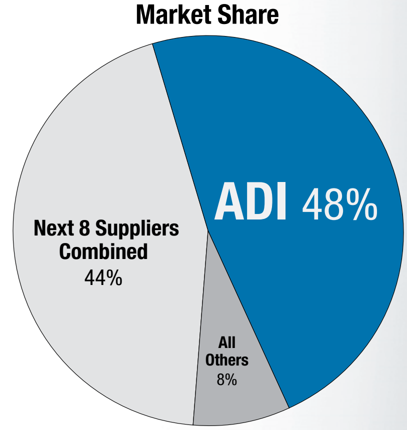

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impossible. Like all things analog, it involves a trade-off. Perhaps you can use a cheaper ADC and better analog components to feed the converter. Then again, it may be better to use a more expensive converter and cheaper analog components. If you are lucky, you can use an inexpensive converter and inexpensive components and calibrate out all the errors with software. In any event, you must examine, analyze, and tabulate the errors in the signal chain so that the trade-offs you make ultimately yield a feasible design.

Component tolerances are fundamental sources of errors. You must analyze and understand how component tolerances affect your input attenuator and other circuits (see **sidebar** "Component tolerances").

FIRST ANALYZE DC ERRORS

Once you understand the dc and ac errors that the input attenuator contributes, you can look at the rest of the signal chain. The input multiplexer can contribute dc errors due to the small on-resistance of the internal semiconductor switches in the part. The on-resistance appears in series with the input resistor to the amplifier, creating an error term. The leakage from the multiplexer channels that are off also add a dc error. The multiplexer and the loading on the input attenuator cause errors, so you must tailor the input impedance of the first amplifier to minimize these errors. The resistor values of the first amplifier can cause issues that create more errors.

An amplifier causes dc errors that come from the imperfect nature of real-world op amps (**Figure 2**). The resistor values are used to set the closed-loop noise gain, which multiplies the op amp's offset-voltage error that appears at the output (**Reference 1**). For noninverting-amplifier configurations, the noise gain equals the closed-loop gain. For inverting configurations, the noise gain equals the closed-loop gain plus one.

The bias current that enters or exits the input pins also creates an error. When you analyze the input bias error, remember that the op amp is in the circuit and is working. As a result, the input bias current reacts to the source resistor, but the op amp servos the voltage that the current creates to keep the input pins of the amplifier at the same voltage. The op amp maintains a constant voltage across the input resistor, so the output error due to input bias current is purely a function of the feedback resistance times the bias cur-

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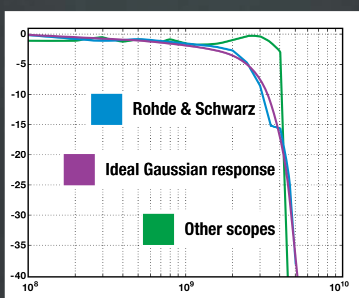
Scope Lie #1

Your digital scope's bandwidth

When it comes to small signal bandwidth, engineers need a gradual signal roll-off to avoid seeing a lot of ringing and overshoot in the time domain.



Today's digital scopes employ very sharp, high-order frequency responses that trade minimum sampling rates for maximum bandwidth. The result is high overshoot and ringing when measuring typical digital signals.

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rent. The resulting voltage error appears at the output in both inverting- and noninverting-amplifier configurations. Derivations for differential amplifiers are a bit more involved and are less apparent (**Reference 2**).

How accurately you scale a signal to your intended gain can also create a dc error. You can refer to published resources to see how a gain error occurs; the open-loop gain of any op amp is not infinite (**Reference 3**). The results of the analysis may also surprise you when you see how significantly large errors can creep into your design. You can derive the gain error as a function of the difference in the ratio, N, between the open- and the closed-loop gain, as the following **equation** shows:

$$\delta=1-\frac{N}{1+N}=\frac{1}{1+N}.$$

Thus, if only a 20-dB difference exists between the open- and the closed-loop gain, N equals 10, meaning that gain error is 9.1% (**Reference 4**). Your error spreadsheet should have a term for this error. Older parts, such as Texas Instrument's LM741 op amp, have minimum open-loop gains of only 10,000 over temperature. In this case, the IC designers provided some good specs at the expense of others. Your application's requirements determine which specs are most important.

Gain nonlinearity also causes measurement errors and is more difficult to characterize and incorporate in an error budget. If the manufacturer of the part you are using does not define gain nonlinearity, you may need to characterize a batch of parts (**Figure 3** and **Reference 5**).

Using op amps in a noninverting arrangement can cause common-mode errors. The common-mode voltage appears on both input pins in common relative to the power-supply rails. Op amps create the least error when

TABLE 1 SLOW- AND FAST-CHANNEL ERROR COUNTS

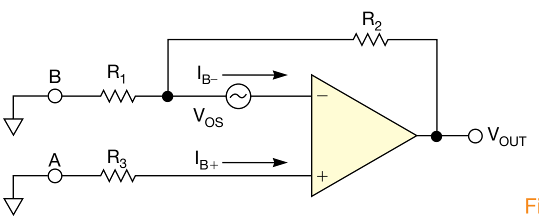
	Slow channel (counts)	**Fast channel** (counts)
Input attenuator	0	0
Buffer amplifiers	0	0
Multiplexer	0	0
First PGA	4	4
Filter	NA	NA
Second PGA	0.2	0.2
Level shift	4.1	0
ADC	NA	NA
Total	8.3	4.2
Maximum allowed	28	28
Margin	19.7	23.8

TABLE 2 OFFSET ERROR

Input voltage (V)	**Attenuator accuracy** (%)	**Attenuator common-mode voltage** (V)	**Buffer amplifiers** (%)	**Multiplexers** (%)	**First PGA** (%)
100	0.01	0.2	0	0	0.1
50	0.01	0.2	0	0	0.1
20	0.01	0.2	0	0	0.1
10	0.008	0.16	0	0	0.1
5	0.008	0.16	0	0	0.1
2	0.008	0.16	0	0	0.1
1	0.008	0.16	0	0	0.1
0.5	0.008	0.16	0	0	0.1
0.2	0.008	0.16	0	0	0.1
0.1	0.008	0.16	0	0	0.1

the input pins are in the center of the power rails. As the input pins approach either rail, an error occurs in the output (**Figure 4**). "Think of it as a worsening of the offset voltage as you sweep the input pins toward either rail," says Paul Grohe, an amplifier-application engineer at Texas Instruments. That offset acts just like the inherent offset voltage: The noise gain multiplies it, and it appears at the output.

Although some manufacturers publish charts that show CMRR (common-mode-rejection ratio) as a function of common-mode input voltage (**Figure 5**), Linear Technology provides graphs for bias current versus common-mode voltage, according to Tim Regan, an amplifier-application manager at the company. These graphs show the effects of common-mode limits versus temperature. Rail-to-rail parts have a guaranteed CMRR with common-mode voltage all the way to either power



$$\text{OFFSET (RTO)}=V_{OS}\left[1+\frac{R_2}{R_1}\right]+I_{B+}\times R_3\left[1+\frac{R_2}{R_1}\right]-I_{B-}\times R_2.$$

$$\text{OFFSET (RTI)}=V_{OS}+I_{B+}\times R_3-I_{B-}\left[\frac{R_1\times R_2}{R_1+R_2}\right].$$

Figure 2 You can calculate offset errors referred to the output or the input pins of the amplifier (courtesy Analog Devices).

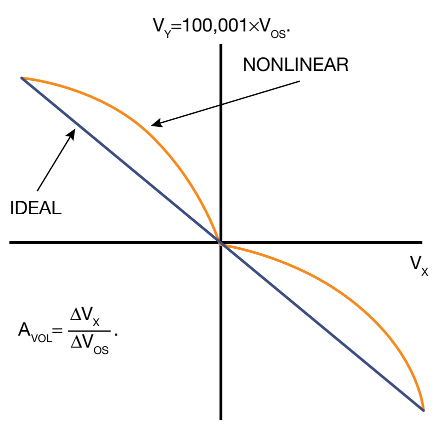


Figure 3 Gain nonlinearity shows up as an error between input V_Y and the amplifier's output, V_X (courtesy Analog Devices).

	Filter (%)	Second PGA (%)	Level shifter (%)	Reference (%)	ADC (%)	Total (%)	Spec (%)
	0.01	0.1	0	0.1	0.02	0.54	0.5
	0.01	0.1	0	0.1	0.02	0.54	0.5
	0.01	0.1	0	0.1	0.02	0.54	0.5
	0.01	0.1	0	0.1	0.02	0.498	0.5
	0.01	0.1	0	0.1	0.02	0.498	1
	0.01	0.1	0	0.1	0.02	0.498	1
	0.01	0.1	0	0.1	0.02	0.498	1
	0.01	0.1	0	0.1	0.02	0.498	1
	0.01	0.1	0	0.1	0.02	0.498	1
	0.01	0.1	0	0.1	0.02	0.498	1

Scope Lie #2
Your digital scope's noise specification

Today's digital scopes only provide a 5 or 10mV/division setting and use a digital zoom to "get down to" a 1mV/division setting. This tactic significantly increases noise while lowering the accuracy. As a way to reduce the noise, some oscilloscopes limit bandwidth on low volts per division settings, while others do not offer the 1mV/division setting at all.

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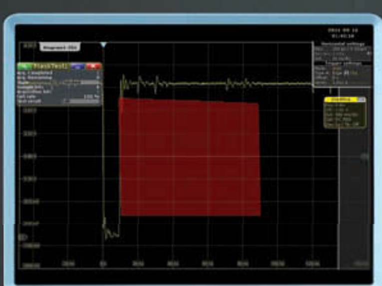
Scope Lie #3

Your digital scope's update rate

Digital scope manufacturers boast update rates of 1+ million waveforms/sec, but this spec excludes measurements and mask testing. These demanding scope measurement tests slow down the update rate of most digital oscilloscopes. When conducting a mask test at lower update rates, finding an event that occurs once per second could take anywhere from minutes to hours.



Try the scope that maintains extremely high waveform update rates while performing a mask test, and locates the error in less than 30 seconds.

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AC ERRORS ARE MORE SUBTLE, MORE DIFFICULT TO UNDERSTAND, AND MORE SERIOUS, ESPECIALLY FOR SIGNAL CHAINS IN 'SCOPES.

rail. For the parts that operate over the rails, such as the LT1638 op amp, the company guarantees the common-mode voltage even above the positive supply. For purpose-built, high-side-current-sense amplifiers, such as the LTC6101, Linear doesn't even spec CMRR, says Regan. Instead, the company provides a PSRR (power-supply-rejection-ratio) spec—the amount of change in the power-supply voltage—because the inputs connect to the positive supply, and they all move together.

Input offsets, bias currents, gain errors, PSRR, and common-mode errors are just a few of the specs that create dc error in your system. The antialiasing filter may cause similar errors if it uses op amps in active configurations. The level-shifting amplifier, which also serves as a buffer for the ADC, also has most of these error terms. Because the first amplifier in the signal chain amplifies the signal, the errors of the filter and the level-shifting amplifier tend to contribute less to total system error, but you still must account for them in your error budget.

When you finally get to the ADC, you can look at the dc specs, such as integral linearity and monotonicity. The ADC's internal or external reference also has dc errors that must be included in your budget. It's usually a good idea and worth the expense to use a high-quality reference because doing so eliminates the need for factory calibrations or any subsequent field adjustments. Potentiometers and trimmers have low reliability, so you may want to incorporate digital potentiometers or DACs to perform the trimming instead of using a mechanical part.

AC ERRORS COME NEXT

Understanding and tabulating all of the dc errors in the analog-signal path are complex tasks, but ac errors are even more subtle, more difficult to understand, and more serious, especially for signal chains such as those in oscilloscopes. Errors on the ac component of a signal occur at all points in the analog-signal chain. Your circuitry also has ac-error sources in the clock circuit that operates the ADC. Just as daunting, errors in the signal can result from the presence of ac

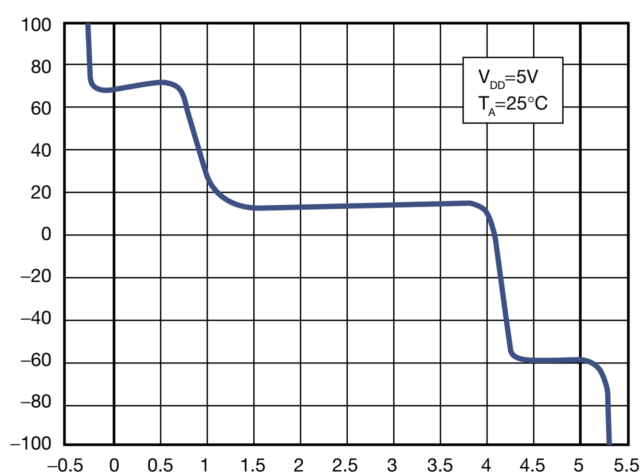

Figure 4 Like most other rail-to-rail-input parts, the TLV2450 amplifier has a dual differential-pair front end, causing the offset voltage and the offset current to change with common-mode input voltage (courtesy Texas Instruments).

noise on the power-supply circuits that feed analog chips.

It helps to look at the error sources from the outputs to the circuit's input. The last analog IC in the signal path is usually an ADC. Examine its ac specs to see whether it can meet your application's needs as it operates as an ac-sampling system on the ac signal.

One key spec is the ADC's ENOB (effective number of bits) at a given sampling frequency. For accurate 10-bit measurements, start with a converter that has an ENOB greater than 10. Otherwise, the rest of the signal chain will further degrade the 10-bit accuracy. Ensure that the converter's bandwidth is as high as the highest frequencies you need to accurately measure. ENOB is a simple way for manufacturers to express the ADC's SNR (signal-to-noise ratio) during operation. You may want to look at pin-compatible converters that come in 12-, 14-, and 16-bit versions so that your board's layout remains the same even if you have to increase the number of bits in the converter.

A buffer and a level-shifting circuit

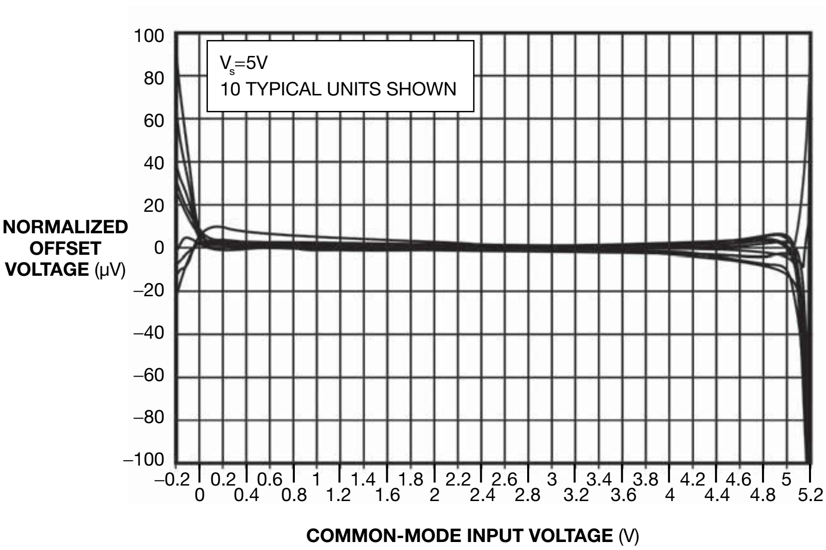

Figure 5 The OPA369 amplifier uses a charge-pump front end, reducing the offset-voltage change over the common-mode input voltage (courtesy Texas Instruments).

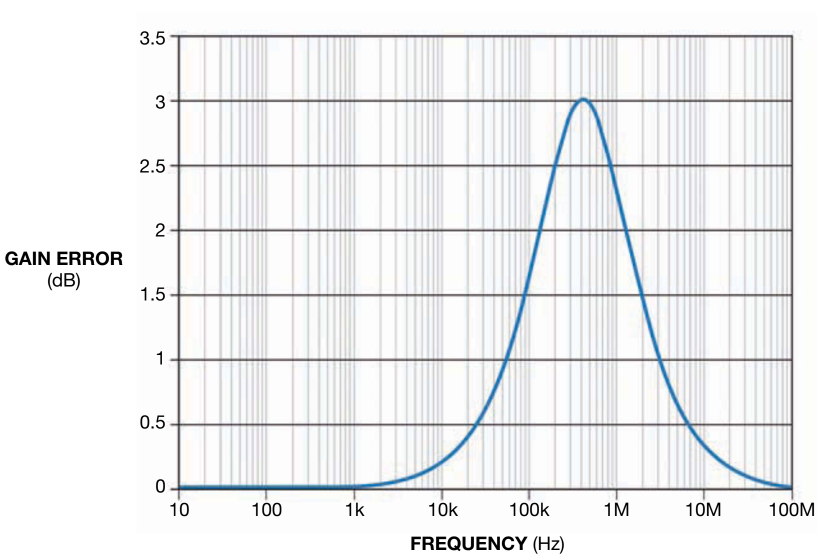

Figure 6 A significant gain error occurs over frequency because an amplifier's open-loop gain rolls off at higher frequencies (courtesy Texas Instruments).

Scope Lie #4

Your digital scope's analog trigger

Most analog and digital scopes utilize separate circuits for trigger and waveform acquisition. These circuits have different bandwidths, varying sensitivities and diverse characteristics which can cause trigger jitter.

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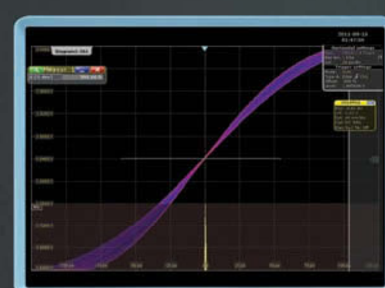

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COMPONENT TOLERANCES

Resistor tolerances in input attenuators create dc errors, and capacitors in the attenuators create a significant amount of ac errors (Figure A). For this reason, you must use discrete capacitors in the input attenuator to swamp out all the stray capacitance in the PCB (printed-circuit board) and in the multiplexer's input pins. Placing three capacitors in parallel with the resistors makes an ac-voltage divider alongside the dc-voltage divider that the resistors create. The capacitor ladder lowers the input impedance at higher frequencies. You must evaluate whether that lower impedance will cause a problem in your measurement system. If so, you must design a different input-attenuator structure. No matter what input structure you use, you must calibrate out the stray-capacitance-induced ac errors. For this reason, it is difficult to achieve both high-impedance inputs and high ac accuracy.

A Monte Carlo Spice simulation of the input attenuator shows serious ac errors in the attenuator at low frequencies (Figure B). You might think that picofarads of capacitance would not make much difference, but they make a big difference at megahertz frequencies. This high-impedance input structure has nominal 1-MΩ input impedance. It takes little capacitor tolerance to create significant errors, and those errors double the nominal dc-error terms at frequencies as low as 2 kHz (Figure C).

Other results of using an input attenuator are less intuitive. You don't necessarily need to use 0.1%-tolerant resistors to achieve a 0.1%-accurate output. A large difference in resistor values means that the tolerance of the larger-value resistor will dominate the output accuracy. Think of a voltage divider with a 100,000-to-1 difference. You could fashion this voltage ladder with a 10Ω resistor and a 999,990Ω resistor. You could use a 0.1%-tolerant resistor for the 999,990Ω resistor and a 1%-accurate resistor for the 10Ω resistor. Nevertheless, the output accuracy remains so close to 0.1% that you can round it to 0.1%. A 50%-accurate voltage ladder with equal-value resistors does require 0.1%-tolerant resistors to ensure a 0.1%-tolerant output voltage.

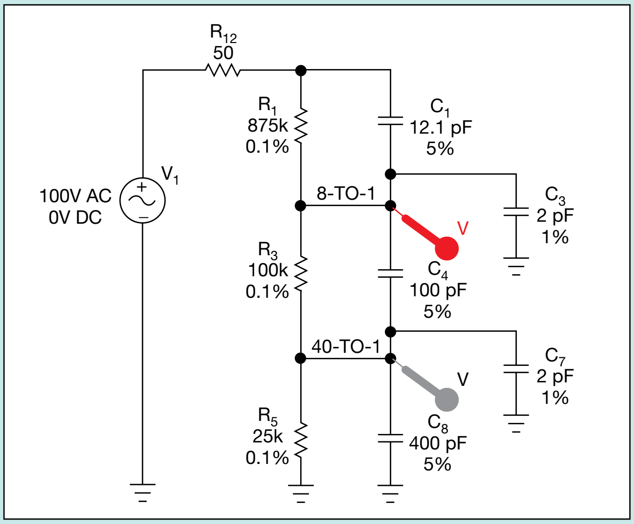

Figure A You can model your input attenuator network in Cadence's Orcad Capture for a Spice simulation. R_{12} is the source resistance of your signal. Discrete capacitors C_1, C_4, and C_8 comprise an ac divider. C_3 and C_7 represent the PCB's and ICs' stray capacitance.

Vendors make resistors with laser trimming for tight tolerances; 1%-tolerant resistors are commonplace, and 0.1%-tolerant resistors are available. To get tighter tolerances, you can use custom resistors on ceramic substrates, such as those from Vishay and BI Technologies. This approach allows you to put multiple thin-film resistors on one substrate; the resistors then track each other over temperature. You can specify thin-film resistors on a single ceramic substrate that track each other to within 0.02%. The absolute-value tolerance of the resistors is 0.05%. This tolerance figure should not pose a problem because you should design your measurement channel so that the ratio of resistors determines a measurement attenuation or gain.

Thin-film ceramic resistors can achieve tighter ratiometric tolerances, such as 0.01%, but cost becomes a factor. Instead, you might investigate using an IC that has built-in resistors, such as those from Linear Technology, Maxim, and Analog Devices. Bear in mind, however, that you cannot just blindly accept the tolerance ranges on the data sheet. You must solder a statistically significant batch of parts onto your PCB and determine whether your soldering process degrades resistor tolerance. If assembling the PCB into an enclosure causes stress or warping, these problems also affect the tolerances of all of the resistors on your PCB, even those inside an IC.

An error-budget spreadsheet is just a nominal starting point to add up all the inaccuracy in your signal path. If the worst-case resistor tolerance goes from 0.2 to 0.3% after soldering, then you must use the 0.3% value in your spreadsheet.

Manufacturers can trim carbon and metal-film resistors—but not carbon-composition or wire-wound devices—during manufacturing. They can measure carbon and wire-wound types only after manufacturing; they then separate the resistors into tolerance bins (Reference A), creating an unusual situation (Figure D). With 10 or 20 carbon-composition resistors in a signal chain, you might think that the entire signal path will have a gaussian distribution of accuracy. Unless you use the most accurate grade a manufacturer offers, however, this scenario is unrealistic because the vendor makes all the resistors in a batch, measures them, puts all of the 1%-tolerant resistors into a bin, and sells them for a higher price. As a result, you cannot count on any resistors in the 5%- or 10%-tolerant line to be the exact value that you want. The vendor removes all of the close-tolerance resistors to sell as 1%-tolerant parts.

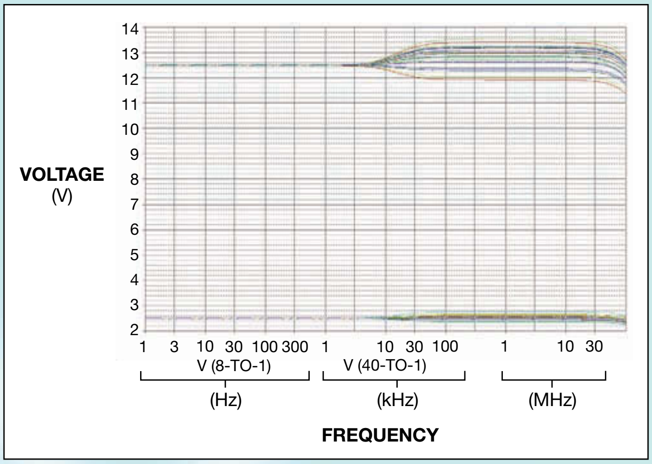

Figure B The PSpice Monte Carlo simulation of the input attenuator shows significant ac errors as low as 10 kHz.

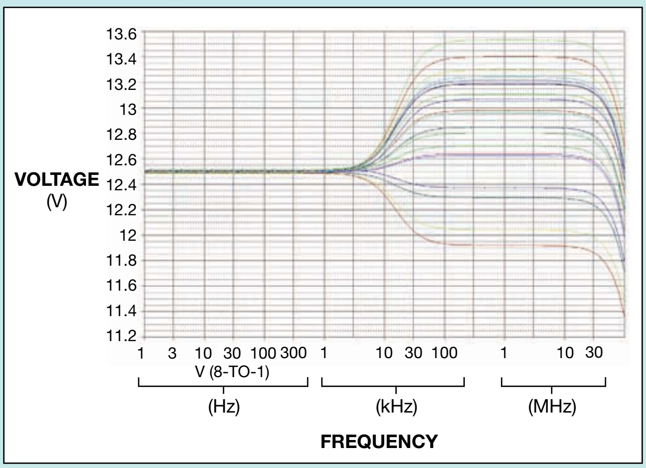

Figure C This expanded view of the simulation demonstrates the difficulty of high-impedance measurement inputs. Even the capacitors' small tolerance changes greatly affect the accuracy at frequencies as low as 3 kHz. Attenuator capacitances react with the source impedance to corrupt measurements at frequencies higher than 30 MHz.

Hence, the distribution of resistor values in the 10% line is not gaussian; it is more like a bathtub distribution with parts that are greater than 5% at a high level and those lower than 5% at a low level. All of the parts are within 10%, but this skewed distribution means that the measurement chain almost never averages out to a tolerance nearing 0%.

If you only rarely use carbon-composition or wire-wound resistors, this problem may seem unimportant, but it occurs in almost all factory-binned parts. Manufacturers select the close-tolerance parts and sell them for higher prices. This scenario can apply to op amps and other active parts.

Capacitor vendors specify looser tolerances on their parts than those of resistors because the vendors cannot automatically trim capacitors during production. They make film capacitors by winding a roll of film into a cylindrical shape. They can precisely control the area of the film, but the thickness of the film varies slightly due to the exigencies and vicissitudes of manufacturing. Film-capacitor vendors just roll up the capacitors and measure them so that they can place them into 10%-, 5%-, and 1%-tolerant bins. Manufacturers of carbon-composition and wire-wound resistors face a similar problem.

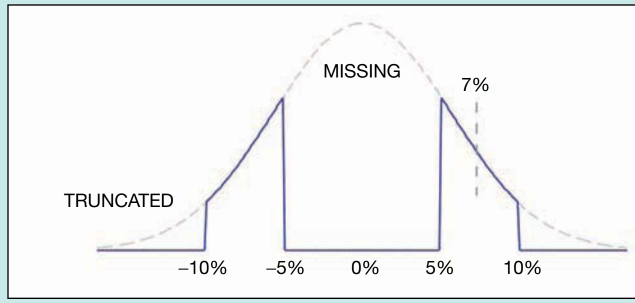

Figure D Manufacturers bin components and ICs in tolerance levels, removing the low-tolerance parts and selling them at higher grades (courtesy Howard Johnson, PhD).

Ceramic capacitors have similar manufacturing variability. Ceramic-capacitor vendors can control the area and layers of the parts but not the distance between the plates of the capacitor after sintering in a high-temperature oven.

Semiconductor junctions form capacitors in a signal chain and behave as varactors. Their capacitance changes depending on the amplitude of the applied voltage, much like a tuning capacitor in a radio. The varying capacitance changes the ac error in your system depending on the signal that is passing through. It can be difficult to minimize these errors and may require you to add compensation components or remove the errors in software.

Inductors are as problematic as capacitors. You must manually select any magnetic inductor to get 1% tolerance. If you are designing high-frequency circuits with air-core inductors, you might be able to ensure that the inductors you buy have tight tolerance, but these parts also cost more than 5%- or 10%-accurate parts.

The fact that precision resistors are much less expensive than precision capacitors and inductors will affect your design choices. Use tighter-value resistors if it allows you to loosen the spec on your capacitors and inductors. Accurate resistors often cost 10 times less than accurate inductors and capacitors. Avoid using mechanical potentiometers or trimming capacitors. After electrolytic and tantalum capacitors, these parts are the least reliable in electronic systems. AVX and Johanson Technology make capacitors you can laser-trim during manufacturing. Their reliability is similar to that of a conventional ceramic capacitor.

REFERENCE

A Johnson, Howard, "7% solution," *EDN*, June 10, 2010, pg 22, http://bit.ly/p14yVv.

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sit just in front of the ADC. The nonideal op amp in this functional block creates ac errors. The dc-gain-error analysis shows that the ratio between open- and closed-loop gain creates substantial gain errors. These errors become worse at higher frequencies because of single-pole gain roll-off, in which the open-loop gain falls to one at the unity-gain-bandwidth point. So the faster you operate any operational amplifier, the less gain ratio there is between the open-loop and the closed-loop gain. You must factor this frequency-dependent error term into your error budget.

Several published sources exist for ac analysis (**references 6** and **7**). If your application requires an accurate signal path, you must use op amps with significantly more bandwidth than your signals. Some designers dispense with amplifiers and instead couple and level-shift with a balun (balanced-unbalanced) transformer. Amplifiers exhibit significant amounts of closed-loop gain error when you feed them signals with frequency components near the unity-gain point (**Figure 6**).

EVERY PIECE OF TEST EQUIPMENT IN YOUR LAB HAS A CALIBRATION SCHEDULE. YOU SHOULD ALSO PROVIDE YOUR OWN CALIBRATION.

THE JOYS OF CALIBRATION

All of the dc and ac error sources combine with spec drift over time to reduce the accuracy of your measurements. For that reason, every piece of test equipment in your lab has a calibration schedule from the manufacturer. You should also provide your own calibration for your designs. "Calibration absolves a lot of sins," says Texas Instruments' Grohe.

The first calibration takes place in the factory during manufacture. This calibration may involve hand-selecting components to meet tighter accuracy specs than the vendor guarantees in the data sheet. Another facet of ensuring accuracy in manufacturing is burning in key components for hundreds or even thousands of hours so that any initial drift occurs before you install the part in your system. Fluke, Agilent Technologies, and Tektronix all perform this task with voltage references that they use in their high-accuracy voltmeters. They solder their reference ICs onto carrier boards or into the main PCBs. They then apply power to the chip until the part's initial drift has settled to a final value. Determining an adequate time for this initial drift to run its course is a science unto itself. Test-equipment manufacturers keep long-term records of various reference ICs they sample from production. IC manufacturers cannot perform a die reduction or a process change without notifying the test-equipment manufacturer. Test companies also buy references from vendors they are not using in production to see whether their data sheets' drift claims are realistic.

Providing an accurate signal chain is difficult, especially in high-impedance systems. One way to handle the problem is to use an analog front end to interface with the sensors in your design. Texas Instruments' LMP91000 analog front end, for example, handles high-impedance inputs and performs signal conditioning and calibration. The company's LMP90xxx and Maxim's MAX1457 family handle resistive-bridge sensors and perform excitation and measurement. ZMDI's ZSI21013 analog front end, like Maxim's parts, performs linearization using an integrated EEPROM. For inductive sensors, you might consider Microchip's MCP2036. Maxim, Analog Devices, and Intersil offer analog front ends for image sensing, and Irvine Sensors' MS3110 capacitance-sensor IC can resolve to capacitances as low as attofarads and has an on-chip EEPROM to store trimming and program settings. The e2v CPIC2.0 for MEMS (microelectromechanical-system) transducers has 30-aF resolution, and austriamicrosystems' AS1716 capacitive-sensor front end senses

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automotive-engine knock. Dozens of capacitive-sensor front ends target touch-sensing applications.

If an analog-front-end IC does not meet your needs, your design should provide for self-calibration wherever possible. Place a ground or a system common in the multiplexer and in the reference voltage and send the reference voltage into one of the multiplexer's channels. You may also want to send one or two key analog power-supply voltages into the multiplexer so that your product's software can apply known voltages and the system can measure its own power supply to calibrate out any errors. With an accurate voltage reference and clock, you know voltage and time. With accurate components for these two characteristics, you can derive other quantities, such as current, resistance, and slew rate. By carefully selecting your components, and using factory and field calibrations, you can keep your signal chain honest and trustworthy.EDN

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BY MARK CANTRELL • ANALOG DEVICES INC

Use reinforced isolation for effective data couplers

UNDERSTAND THE REQUIREMENTS AND MANDATES FOR ELECTRIC-SHOCK SAFETY WITH RESPECT TO THIS COMMON COMPONENT.

The primary tenet of electric-shock safety is that the equivalent of two independent insulation systems must lie between dangerously energized circuits and any conductor that a user of an electrical device can access. One of these insulation systems could be a safety-grounded enclosure with a single layer of internal insulation. Another approach is to use two insulation systems to provide redundant protection.

Complex electrical systems using the double-insulation approach require galvanically isolated communications across two layers of insulation without losing signal integrity. This requirement creates the need for devices with the equivalent electrical strength and reliability of two redundant-insulation systems. The so-called reinforced-insulation device relies on a combination of construction, type testing, and continuous monitoring in production to ensure safety equivalence to two independent systems. This article examines how to achieve reinforced insulation in optocouplers and digital isolators with respect to construction and the test requirements of the IEC's (International Electrotechnical Commission's) IEC60950 and the related IEC60747-5-5 and VDE (Verband der Elektrotechnik, Elektronik und Informationstechnik)-0884-10, as well as differences with other accepted IEC standards for both types of isolators.

SAFETY ISOLATION

Modern systems require isolation to communicate with high-side components in battery-charging systems or motor drives, to break ground loops in communications systems, and to protect users from dangerous line or secondary voltages. The level of safety an application requires determines the level of isolation the application needs.

Functional isolation provides only the insulation necessary for the component to function properly but provides no protection to a user. Basic insulation provides a level of insulation from shock that is adequate for protecting an operator if the insulation is fully intact. However, to protect people from hazardous voltages, regulations require double insulation: the stipulation that two independent insulation systems be present—basic insulation for shock protection and a supplemental layer so that, if a fault breaches one insulation system, a redundant system will still provide safety to the operator. When evaluating insulation systems, the primary requirement is safety, not electrical function, so the failure criterion during evaluation is whether the isolation barrier is intact after the qualification. It is an added bonus if the part still functions to the original specifications.

An example of a reinforced-insulation system is the feedback-control loop in a power supply. Information about the output-voltage level must flow from the SELV (safety-extra-low-voltage) side of the ac/dc converter to the line side of the power supply. Operators can be in contact with the SELV side

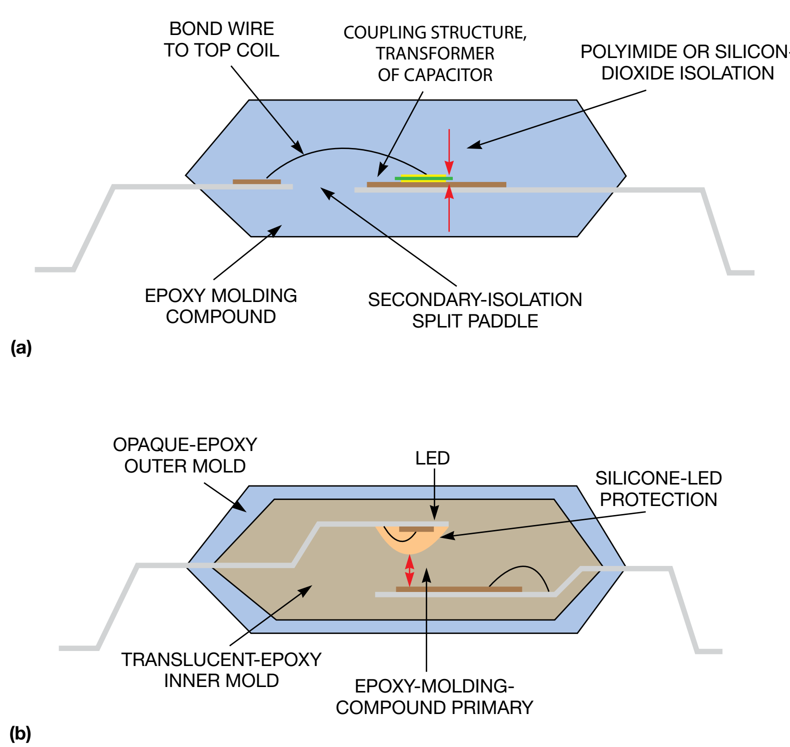

Figure 1 The component structure of both digital-isolator construction (a) and optoisolator construction (b) has reinforced insulation.

TABLE 1 CREEPAGE AND CLEARANCE REQUIREMENTS

AC mains (V rms)	Mains category (V rms)	Class II transient voltage (V rms)	Basic creepage/ clearance (mm)	Reinforced creepage/ clearance (mm)
240	300	2500	2.5/2	5/4
400	600	4000	4/3.2	8/6.4

of the power supply, so two independent isolation systems or a reinforced-insulation system must be present in the datapaths to protect operators from shock.

Passive components, such as resistors or capacitors, can operate in series without significant functional degradation, but putting two data isolators into the path would be impractical for several reasons. First, analog data would lose fidelity, and digital data would have long propagation delays and added jitter. Second, this scenario would create the need for an intermediate power supply to run the coupler interfaces between the two layers of isolation. The impracticality of doubling up data-isolation devices creates the need for components that directly connect across a double-insulation boundary without sacrificing safety. The use of this type of component means that a system has reinforced insulation (**Figure 1**).

COMPONENT-LEVEL REQUIREMENTS

You can evaluate component-reinforced insulation either using the external dimensions of the component, such as creepage, clearance, and tracking index, or using internal electrical performance. Internal and external requirements are handled in very different ways. Creepage is the shortest distance along the surface of a component between electrically isolated conductive structures, such as component pins. Clearance is also the shortest distance between isolated conductive structures in a component, but it need not be on the surface, so the path can jump over grooves and be suspended over ridges.

In simple geometries, the creepage and clearance paths are often the same. **Figure 1** shows the creepage path for a JEDEC Solid State Technology Association standard SOIC (small-outline integrated circuit) because many isolation devices use this style of package. The creepage and clearance for this package have the same path and length. Creepage is always greater than or equal to the clearance. An additional external property of components that is critical to insulation ratings is the CTI (comparative tracking index), a measure of how easily an insulating material will erode under electrical discharge. Higher tracking voltages will allow smaller creepage and still maintain safety.

External dimensions must be equivalent to the total distances that the basic and supplemental layers of a double-insulation system provide. In general, all creepage and clear-

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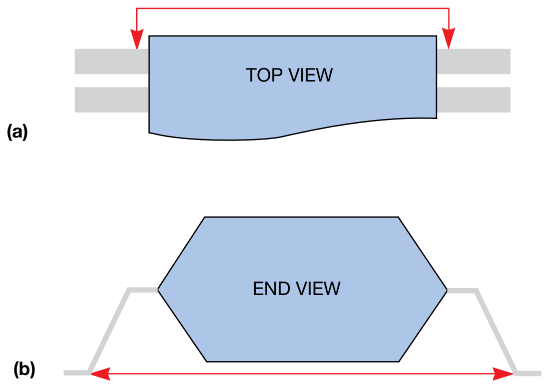

Figure 2 Two common operating conditions show the required package creepage (a) and clearance (b).

ance requirements are twice as large for reinforced components as for basic and supplemental components. **Table 1** and **Figure 2** show two common operating conditions and the required creepage and clearances. With this approach, the external environment and the surface properties determine the external spacing requirements, including the amount of expected contaminants, the air pressure, and tracking: the tendency of surface discharges to erode the outer surface of a component.

For internal properties of components, the quality of the insulation is more important than the quantity or the thickness of the insulation. The manufacturer can demonstrate that the part has the required electrical properties to withstand the voltage stresses in both the long term and the short term. The requirements of the IEC60950 standard are for office and telecom equipment and, to a large extent, for medical devices. You can readily verify the external dimensions and materials with a micrometer and some bulk material testing for a tracking index.

For internal requirements, you can use any of three approaches for qualifying the component. The simplest approach is to evaluate the component as if it contained only solid insulation. This approach requires that all of the internal distances through the insulation or along cemented joints are greater than 0.4 mm. No further type testing is required. However, it is difficult to make a high-performance data coupler that meets these requirements. It is widely believed that the 0.4-mm minimum insulation thickness applies to all reinforced isolation devices, but it does not, and this misconception is a point of confusion for many engineers.

Another approach is to apply the rigorous IEC60747-55 standard, which qualifies optocouplers for reinforced insulation and has a battery of type tests and life tests with isolation-withstand verification tests after each one. This standard currently applies only to optocouplers, not other newer digital isolators; however, VDE has created a draft standard, VDE0884-10, which applies the insulation tests of the IEC60747-5-5 standard to digital isolators.

Alternatively, you can treat the component as a semiconductor device. This category of devices has a set of type tests similar to the IEC60747-5-5 requirements. You use this approach with digital isolators because the testing requirements of the optocoupler standard target use in optocoupler structures.

Qualification to and maintenance of a reinforcement rating is accomplished in three phases. First, you evaluate materials and dimensions and conduct electrical type testing. Testing includes thermal cycling, limited life testing, and electrical overstress that would cause heating or catastrophic insulation failure. The integrity of the isolation is checked with a voltage-withstand test after each environment or test. IEC60747 type testing covers materials tests for CTI and flammability; electrical tests for withstand, partial discharge, insulation resistance, surge, and overload; and mechanical tests for thermal cycle, thermal shock, vibration, high-temperature storage, and creepage and clearance.

After the part receives approval based on its dimensions and type testing, a voltage-withstand test checks insulation integrity for each device during manufacture. IEC60747-5-5 and equivalent certifications perform a partial-discharge insulation-quality test on each device. The certifying body conducts periodic audits to verify that material sets and dimensions have not

changed and that calibrated equipment is properly conducting all assembly-line tests. The auditor may periodically repeat and review a sample of some of the tests.

TRENDS IN ISOLATION REQUIREMENTS

Different standards can have disparate requirements at the component level. One standard may even vary from edition to edition. This trend is becoming less problematic as IEC is moving toward a unified approach. This approach will likely take a significant amount of time to achieve because each standards committee has significant independence. A unifying trend in the application of system-level standards is the availability of component-level standards, such as IEC60747-5-5. If such a standard exists for a component, you can apply it instead of the requirements of a system-level standard.

The IEC and VDE standards set a high bar for reinforced insulation, including surge testing at levels of 10 kV or higher. Thin insulation layers cannot pass this test, which is the discriminating test for many optocouplers and digital isolators for qualification as reinforced insulation. Components that cannot meet the requirements usually fall back to the IEC60747-5-2 standard, which can be applied to basic insulation.

Yet another confusing point for designers of isolated systems is the assumption that an IEC60747-5 qualification automatically confers reinforced status. The IEC committees are currently working to revise the IEC60747-5-5 standard to include digital isolators. The next unified standard will be applicable across all IEC system-level standards and should help to eliminate confusion in the future.

Manufacturers design and qualify reinforced insulation in data isolators to provide the protection of double-insulation systems and the data-transmission performance available with a single isolation barrier. Externally, the components have a creepage and clearance requirement that is twice the basic insulation requirement. Internally, insulation either meets the requirements of solid insulation, including through the insulation minimum distance, or it receives extensive type testing and assembly-line testing during production. The availability of a reinforced insulation rating that is verified by testing rather than detailed structural requirements allows innovation in insulation technology to be qualified without rewriting the standards for each new technology.EDN

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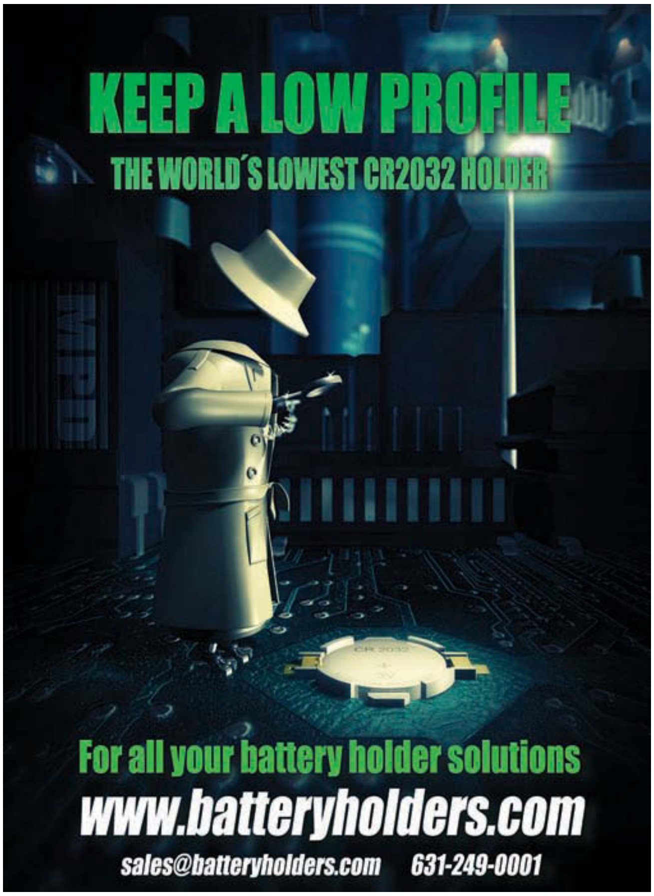

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Use a self-powered op amp to create a low-leakage rectifier

Martin Tomasz, Sageloop Designs, San Francisco, CA

You can combine a carefully chosen op amp, a low-threshold P-channel MOSFET, and two feedback resistors to make a rectifier circuit with less forward drop than a diode (**Figure 1**). The rectified output voltage powers the active circuitry, so no additional power supply is necessary. The circuit's quiescent current is lower than most Schottky diodes' reverse-leakage current. This circuit provides active rectification at voltage drops as low as 0.8V. At lower voltages, the MOSFET's body diode takes over as an ordinary diode.

The op-amp circuit turns on the MOSFET as a forward voltage develops between the input and the output voltages, according to the following **equation**:

$$V_{GATE}=V_{OUT}-(R_2/R_1)(V_{IN}-V_{OUT}),$$

where V_{GATE} is the MOSFET's gate drive, V_{IN} is the input voltage, and V_{OUT} is the output voltage. You can relate the input and the output voltages to the MOSFET's drain-to-source and gate-to-source voltages, according to the following **equations**:

$$V_{DS}=V_{IN}-V_{OUT} \text{ and } V_{GS}=V_{GATE}-V_{OUT},$$

where V_{DS} is the drain-to-source voltage and V_{GS} is the gate-to-source voltage. Combine these **equations** to relate the MOSFET's gate drive to a function of the drain-to-source voltage:

$$V_{GS}=-(R_2/R_1)V_{DS}.$$

If you make R_2 12 times larger in value than R_1, a 40-mV voltage drop across the MOSFET's drain-to-source voltage is sufficient to turn on the MOSFET at low drain currents (**Figure 2**). You could choose a higher ratio to further reduce the voltage drop within the limits of the op amp's worst-case input-offset voltage of 6 mV. The op amp is powered from output-reservoir capacitor C_1. The amplifier has rail-to-rail inputs and outputs and no phase inversion when operating near the rails. The amplifier operates at power-supply voltages as low as 0.8V. You directly connect the op amp's noninverting input to the V_{DD} rail and the amp's output to the gate of the MOSFET. The circuit consumes slightly more than 1 µA when actively rectifying a 100-Hz sine wave, less current leakage than that

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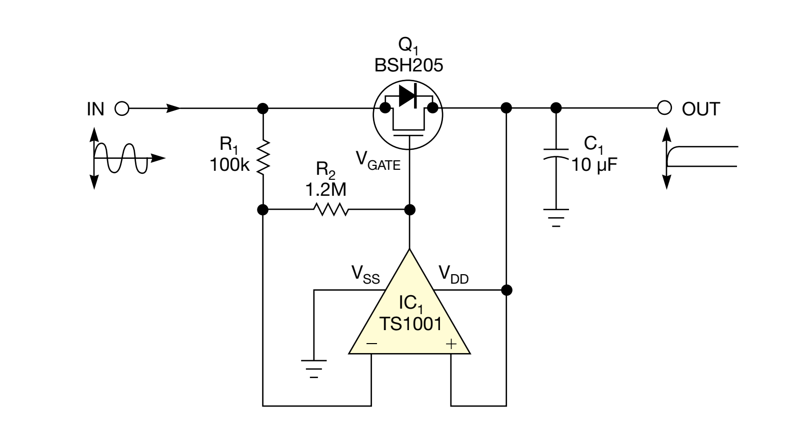

Figure 1 This circuit emulates a rectifier, but it has forward-voltage drop of 40 mV or less. The circuit has less reverse leakage than a Schottky diode.

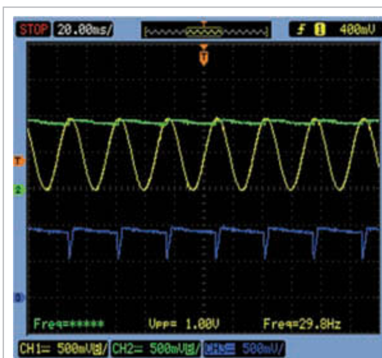

Figure 2 The output of the circuit (green) with a sine-wave input (yellow) shows that the FET's gate voltage (blue) drops out only when the input-to-output differential is less than 40 mV.

of most Schottky diodes. The BSH205 supports milliamp-level currents at a gate-to-source voltage of 0.8V.

The op amp's bandwidth limits the circuit to lower-frequency signals. At bandwidths higher than 500 Hz, the amplifier's gain begins to decline. As the signal frequency increases, the MOSFET remains off, and the body diode of the MOSFET takes over the rectification function. An input with a fast fall time could potentially drag the output with reverse current through the MOSFET. However, for small currents, the MOSFET operates in its subthreshold range. The amplifier quickly turns off due to the exponential relationship of the gate-to-source voltage to the drain-to-source current in the subthreshold range. The limiting factor is the amplifier's slew rate of 1.5V/msec. As long as you don't load the circuit so heavily that you drive the MOSFET into its linear range, reverse currents won't exceed forward currents.

You can use the circuit in a micropower solar-harvesting application (**Figure 3**). Depending on the light, the BPW34 cells generate 10 to 30 µA at 0.8 to 1.5V. The active-diode circuit rectifies the peak harvested voltage in conditions of rapidly changing light and minimizes reverse leakage to the cells. **EDN**

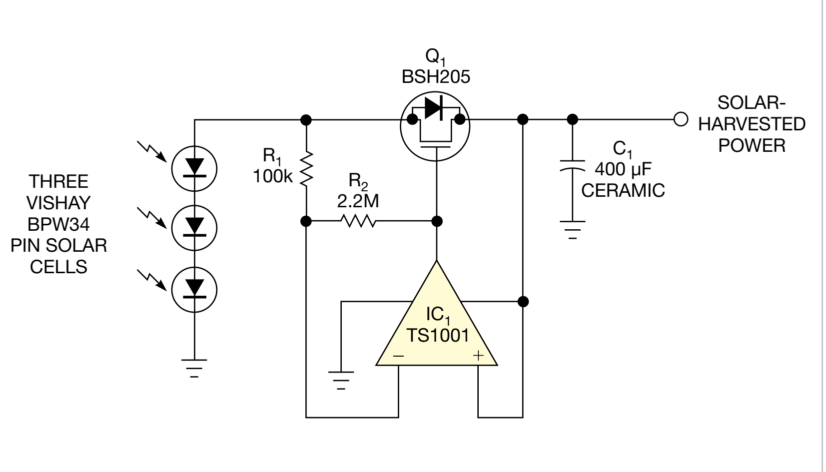

Figure 3 You can use the active-rectifier circuit to charge a capacitor from solar cells. The rectifier has low voltage drop and protects the cells from reverse current when there is no light.

Simple reverse-polarity-protection circuit has no voltage drop

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

Common methods of reverse-voltage protection employ diodes to prevent damage to a circuit. In one approach, a series diode allows current to flow only if the correct polarity is applied (**Figure 1**). You can also use a diode bridge to rectify the input so that your circuit always receives the correct polarity (**Figure 2**). The drawback of these approaches is that they waste power in the voltage drop across the diodes. With an input current of 1A, the circuit in **Figure 1** wastes 0.7W, and the circuit in **Figure 2** wastes 1.4W. This Design Idea suggests a simple method that has no voltage drop or wasted power (**Figure 3**).

Select a relay to operate with the reverse-polarity voltage. For example, use a 12V relay for a 12V supply system. When you apply correct polarity to the circuit, D_1 becomes reverse-biased, and the S_1 relay remains off. Then connect the input- and output-power lines to the normally connected pins of the relay, so current flows to the end circuit. Diode D_1 blocks power to the relay, and the protection circuit dissipates no power.

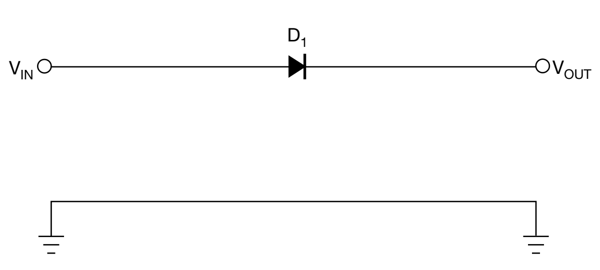

Figure 1 A series diode protects systems from reverse polarity but wastes power in diode losses.

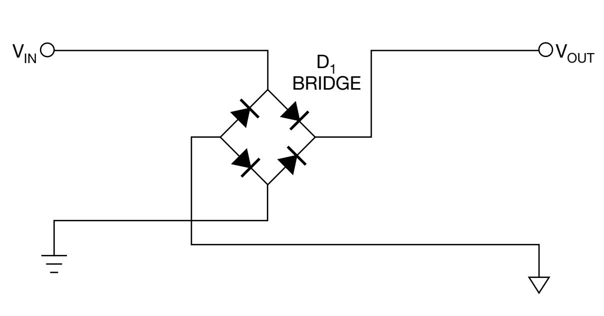

Figure 2 You can use a bridge rectifier so that your system works no matter what the input polarity is. This circuit wastes twice the power, in diode losses, of the circuit in Figure 1.

When you apply incorrect reversed polarity, diode D_1 becomes forward-biased, turning on the relay (**Figure 4**). Turning on the relay cuts the power supply to the end circuit, and red LED D_3 turns on, indicating a reverse voltage. The circuit consumes power only if reverse polarity is applied. Unlike FETs or semiconductor switches, relay contact switches have low on-resistance, meaning that they cause no voltage drop between the input supply and the circuit requiring protection. Thus, the design is suitable for systems with tight voltage margins. EDN

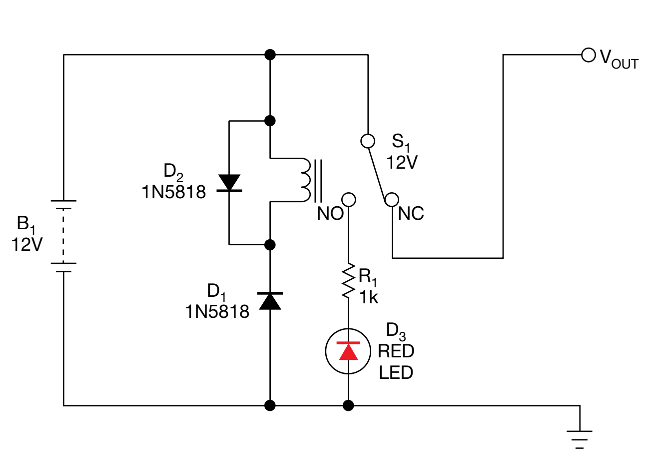

Figure 3 You can wire a relay switch to pass power to your system with no power loss. D_2 clamps inductive kicks from the relay coil.

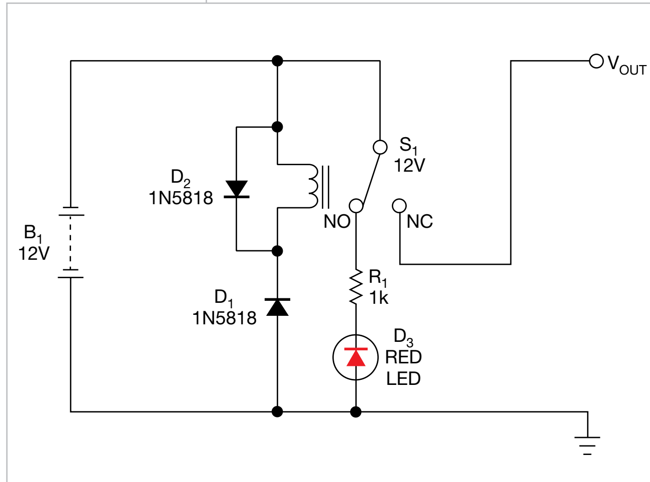

Figure 4 With reversed input voltage, the relay switch engages, interrupting power to the system, and the LED lights.

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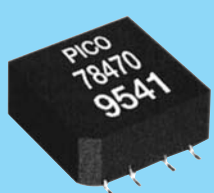

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Series-LC-tank VCO breaks tuning-range records

Louis Vlemincq, Belgacom, Evere, Belgium

This Design Idea applies a novel topology to an oscillator. It uses a series-connected LC (inductive-capacitive) tank circuit to give the circuit a higher tuning range than circuits that use a parallel-LC connection. The architecture of the oscillator permits wide frequency swings, well beyond the capabilities of the best hyperabrupt varactor. Engineers deem a VCO (voltage-controlled oscillator) capable of covering one octave as state of the art. This topology allows a 4-to-1 ratio in output frequency. The LC tank alone sets this frequency so that the parasitic capacitances of other components do not limit the output frequency. Unlike standard oscillators, this circuit works well at its frequency extremes.

At first glance, the central structure of the oscillator resembles two transistors that form a latching SCR (silicon-controlled-rectifier) structure (**Figure 1**). The structure is similar to that of a thyristor, but you add degeneration resistors that keep the circuit in a linear mode of operation. The resistors make the gain of this "SCR" smaller than one, and it is dc-stable. The series-tuned tank circuit increases the gain beyond one at the resonant frequency, causing the circuit to oscillate. No auxiliary components are necessary for oscillation, and the node between the inductor and the capacitor is free of other connections, meaning that only the varactor you use as the capacitor determines the tuning range. The frequency varies as the square root of the tuning elements. To change the frequency by a factor of two, you need a fourfold variation of the tuning capacitance.

Unlike a parallel-LC tank, the resonant current passes through the active element and is, therefore, limited. This limit in turn means that the ac voltage appearing across the tuning components is small—typically, less than 100 mV. The small signal reduces the effects of circuit nonlinearity and the impact of the self-biasing effects of the signal on the varactor. You can use control voltages as small as 0.3V across the varactor. If you use a 1-μH inductor, the circuit still oscillates with capacitor values of 4.7 pF to 4.7 μF—a ratio of 106-to-1.

For the detailed design, move the LC tank to the emitter of PNP transistor Q_2 (**Figure 2**). The lower speed of the PNP creates greater phase difference and encourages oscillation. Connect L_2 and C_2 at a common power point on the power rail, emphasizing

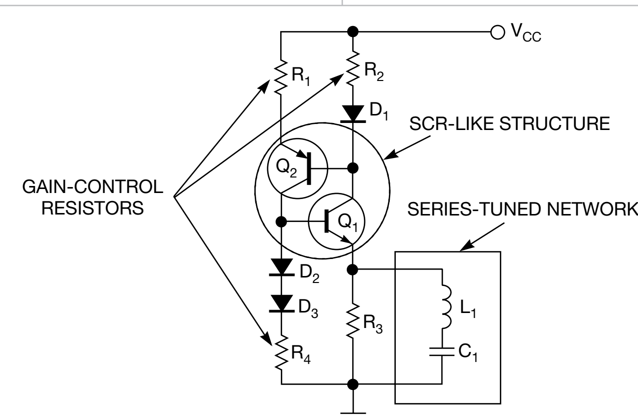

Figure 1 The heart of the oscillator are two transistors and a series-LC tank. The gain-control resistors add degeneration so that the transistors operate in their linear range instead of latching, as an SCR would.

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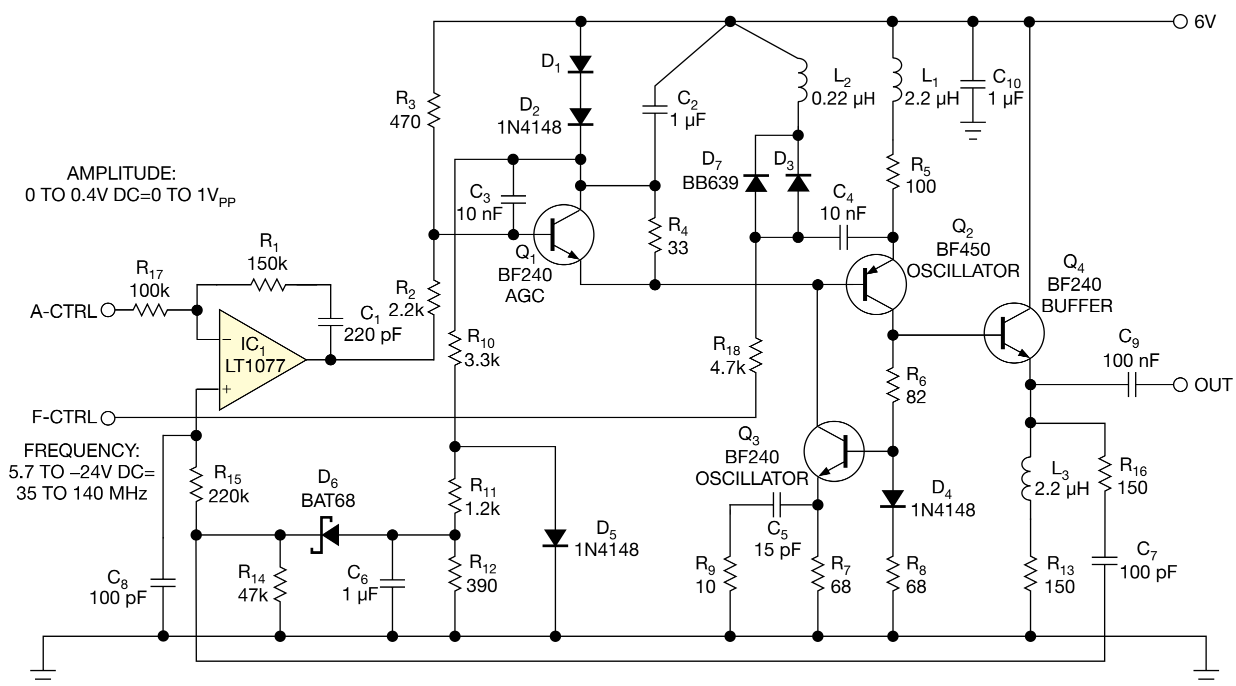

Figure 2 For the detailed design, move the LC tank to the PNP transistor. Varactors D_7 and D_3 form the capacitance, and L_2 is the inductance.

the criticality of the layout in this part of the circuit. The oscillator "senses" the tuned circuit through C_2 and C_4, and anything inside that loop adds uncontrolled parasitics to L_2. These parasitics would compromise the AGC (automatic-gain-control) action and degrade the performance and accuracy of the oscillator.

Q_1 and associated components implement the AGC. A parallel-LC oscillator tolerates clipping of the signal, but this series-LC circuit degenerates into a multivibrator if you allow the signal to grow so large that it clips. The AGC servo action has the added advantage of producing uniform output amplitude. Use D_5 to create a 0.6V dc bias. R_{11} and R_{12} form a voltage ladder that creates a dc-bias voltage close to the forward-voltage drop of Schottky diode D_6. This bias allows D_6 to work as a more perfect rectifier of the small output signal. C_8 integrates the rectified signal into a dc voltage proportional to the amplitude of the circuit's output. Apply this dc signal to IC_1, the AGC amplifier, through a filter comprising R_{15} and C_8. The op amp servo-controls the filtered dc signal against the A-CTRL input-amplitude signal you send to the circuit. This signal allows you to set output amplitude at 0 to 1V.

In this example, the output amplitude is 0.9V. The frequency range extends from 35 to 140 MHz, a 1-to-4 ratio—twice that of conventional high-performance VCOs—and requires a fourfold increase in the capacitance ratio. The overall capacitance ratio is 1-to-16, exactly that of the varactor itself. At the lowest (**Figure 3**) and highest (**Figure 4**) frequencies of the output range, the quality of the sine wave remains excellent, thanks to AGC action. EDN

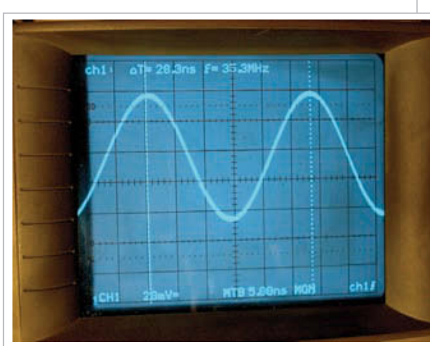

Figure 3 At 35 MHz and 0.9V output, the oscillator creates a high-quality sine wave.

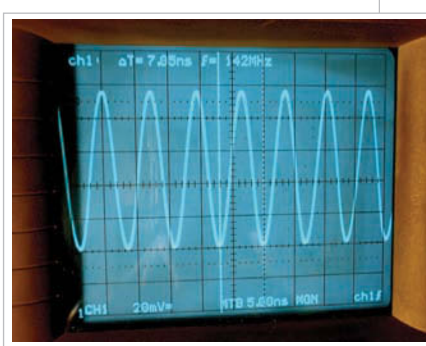

Figure 4 At 142 MHz and 0.9V, the output is still pure and stable, thanks to the AGC circuit.

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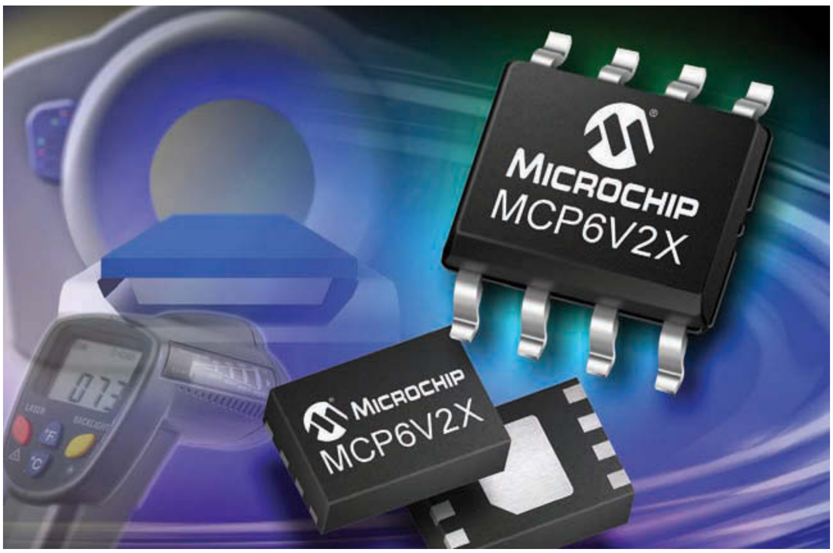
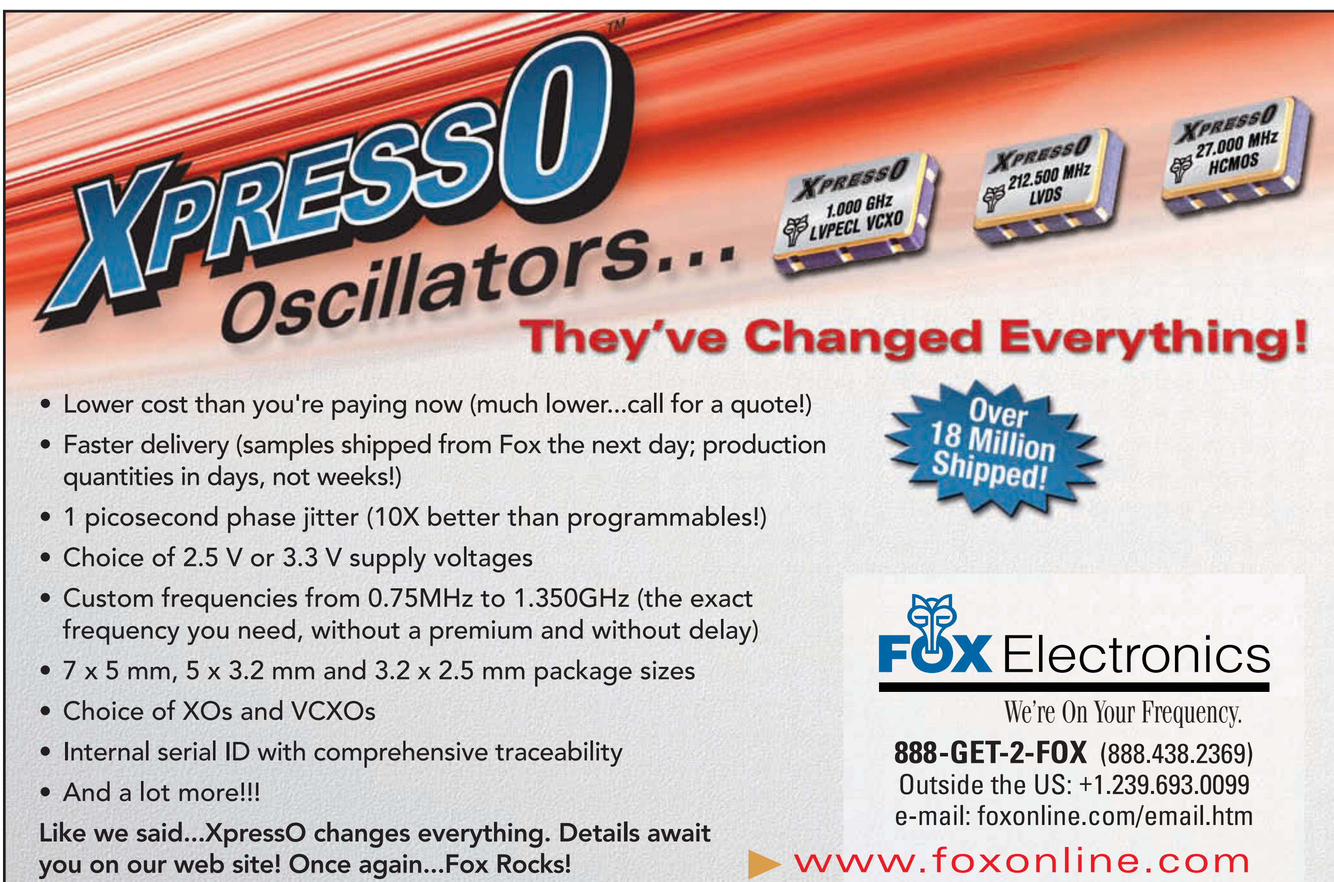


Microchip expands autozero-op-amp line with MCP6V2X family

The MCP6V2X family of op amps features a self-correcting autozero architecture, which enables high precision, including an input offset voltage of 2 μV and a gain-bandwidth product of 2 MHz. With noise of 50 nV/√Hz, the MCP6V2X family has 2.3 to 5.5V operating voltages, and the devices' rail-to-rail I/O structure allows for full-range use, even in low-supply conditions. The devices are available in eight-pin MSOPs and suit use in consumer, industrial, and medical applications. The MCP6V26 and MCP6V28



productroundup

are available in eight-pin SOIC, MSOP, and 2×3-mm TDFN packages and sell for $1.13 and $1.18 (10,000), respectively. The MCP6V27 is available in eight-pin SOIC, MSOP, and 4×4-mm DFN packages for $1.73 (10,000).
Microchip, www.microchip.com

ADI's ADA4096-2 op amp solves precision/ OVP trade-off problem

The ADA4096-2 dual op amp offers high precision along with ±30V of integrated input OVP (overvoltage protection). This level of internal OVP for inputs means that analog designers using the ADA4096-2 can eliminate or minimize the need for external OVP design and components. The op amp targets industrial sensors and other applications needing precision signal handling, high accuracy, and ultralow power consumption. The ADA4096-2 draws 60 μA of power per amplifier and features twice the bandwidth and half the voltage noise of its competitors, according to the vendor. The device sells for $1.87 (1000).

Analog Devices, www.analog.com

TI's 36V OPA2188 op amp touts zero drift

The 36V OPA2188 op amp finds use in high- and low-voltage-supply applications requiring high precision, such as test-and-measurement equipment, electronic weigh scales, medical instrumentation, and flow meters. The device's zero-drift, 0.03-μV/°C architecture reduces the need for future system calibration, and its initial offset voltage of 25 μV enables high-resolution sensor measurements. The OPA2188 provides 2 MHz of bandwidth and consumes 475 μA of quiescent current, providing high accuracy. For high system precision, the device achieves low noise of 8.8 nV/√Hz. An input common-mode range extends from the negative rail to within 1.5V of the positive rail, eliminating the need for additional circuitry and enabling 5V, single-supply operation. The OPA2188 is available in a 3×5-mm MSOP or a 5×6-mm SOIC package for a suggested retail proce of $1.40 (1000).

Texas Instruments, www.ti.com

Linear Tech's LTC6360 op amp drives SAR ADCs to 0V on 5V supply

The LTC6360 op amp drives 16- and 18-bit SAR ADCs. It can drive to 0V and maintain high linearity on a 5V supply through its integrated ultra-low-noise charge pump. Maximum input offset voltage is less than 250 μV, and noise is 2.3 nV/√Hz. The device settles to 16 bits in 150 nsec and achieves a closed-loop −3-dB bandwidth of 250 MHz. Second- and third-harmonic-distortion figures are −103 and −109 dBc, respectively, at an input frequency of 40 kHz. The output drives a series-10Ω-resistor/330-pF-capacitor-filter network and can drive larger load capacitances. The LTC6360 is available in MSOP and 3×3-mm, eight-pin DFN packages and operates over the 0 to 70°C commercial, −40 to +85°C industrial, and −40 to +125°C extended temperature ranges. Prices start at $2.19 (1000).
Linear Technology, www.linear.com

TI's LMH6522 amps target wideband-radio systems

The LMH6522 quad and LMH6521 dual digital variable-gain amps suit use in multichannel wideband wireless systems. The amps feature output-third-order-intercept points of 49 and 48.5 dBm, respectively, at a 200-MHz input frequency. They offer 1- and 0.5-dB gain steps over 31- and 31.5-dB ranges and noise figures of 8.5 and 7.3 dB, respectively, at maximum gain. The LMH6522 and LMH6521 come in 54- and 32-pin LLPs and sell for $9.85 and $6.15 (1000), respectively.
Texas Instruments, www.ti.com

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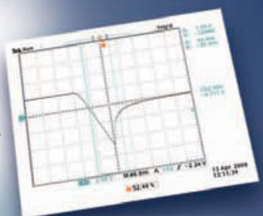

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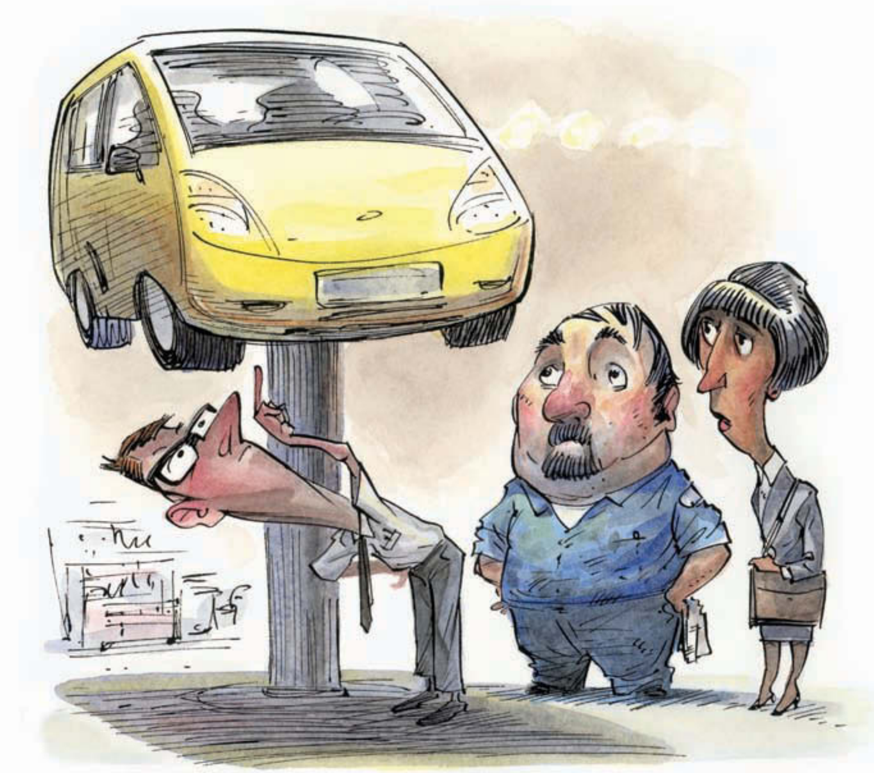

DANIEL VASCONCELLOS

EMI/EMC (electromagnetic-interference/electromagnetic-compatibility) certification is among the toughest design milestones for embedded automotive controllers. My company once developed an 8-bit controller for air-path control of a direct-injection diesel engine. Engine-performance results were encouraging, so the next step was to approach the local certification agency for EMI/EMC-compliance testing. The EMI test was a piece of cake: An onboard 4-MHz crystal generated almost no RF interference.

As the engineer switched on the EMC chamber, we were almost certain that the unit would valiantly withstand the onslaught of strong RF radiation. When the controller reached 50 MHz, however, all of the outputs then turned off.

Suspecting a software error due to intense radiation, I checked the microcontroller's output pins. They were showing dead-on accurate logic levels. This finding pointed the needle of suspicion toward the Infineon TLE 6216 output chip. I couldn't believe that the chip would fail under EMC testing. When we withdrew the EMC-test radiations, the outputs remained off. Apparently, they tripped due to an internal short circuit. As we power-cycled the controller, the outputs regained their correct logic levels. However, when EMC radiation was restored, the outputs immediately tripped again.

Postponing the EMC test until the next day, we took the unit to our laboratory for analysis. The chip outputs included RF-filter capacitors near the field connector.

I understand the purpose of RF input capacitors, but I have never believed that they should be near the power-output pins. I found it hard to believe that EMC radiation would corrupt low-impedance, high-power outputs. Nevertheless, we were religiously placing those capacitors, according to standard automotive-design tenets, at all field connections.

In view of our earlier problems, I checked the ground tracks of the capacitors. They terminated on a separate RF ground. However, RF ground and signal ground were supposed to connect through a small jumper near the power connector, but this prototype unit had a dry-soldered power connector. This finding answered my question regarding the role of the output capacitors: These output pins also included input circuits to sense overcurrents and short circuits to activate internal trip circuits for protection. EMC radiation can corrupt these input circuits, thus tripping the protection circuits.

We rectified the dry-solder problem and continued the test on the next day. This time, the output chip did not trip at all and obediently followed CPU commands for most of the frequencies from 1 to 400 MHz. However, the outputs were erratically tripping at frequencies higher than 400 MHz. Apparently, the low-cost filter capacitors that automotive applications typically use were not up to the task at those frequencies.

I also reviewed designs of other units we had developed that had passed this test. Most of them used output chips with short-circuit limits, which we could program through an SPI (serial-peripheral interface), such as an STMicroelectronics L9823 octal low-side driver. This driver would never cause an IC to trip its outputs during EMI and EMC testing. Using such a chip would have meant lengthy software and hardware modifications. Instead, we inserted inductive-bead filters in the output lines to suppress the high frequencies that were troubling us during the test. This measure was successfully able to guard all of our outputs from spurious tripping during the next EMC tests a few months later. EDN

Vishwas Vaidya heads an embedded-design team at Tata Motors (Pune, India).

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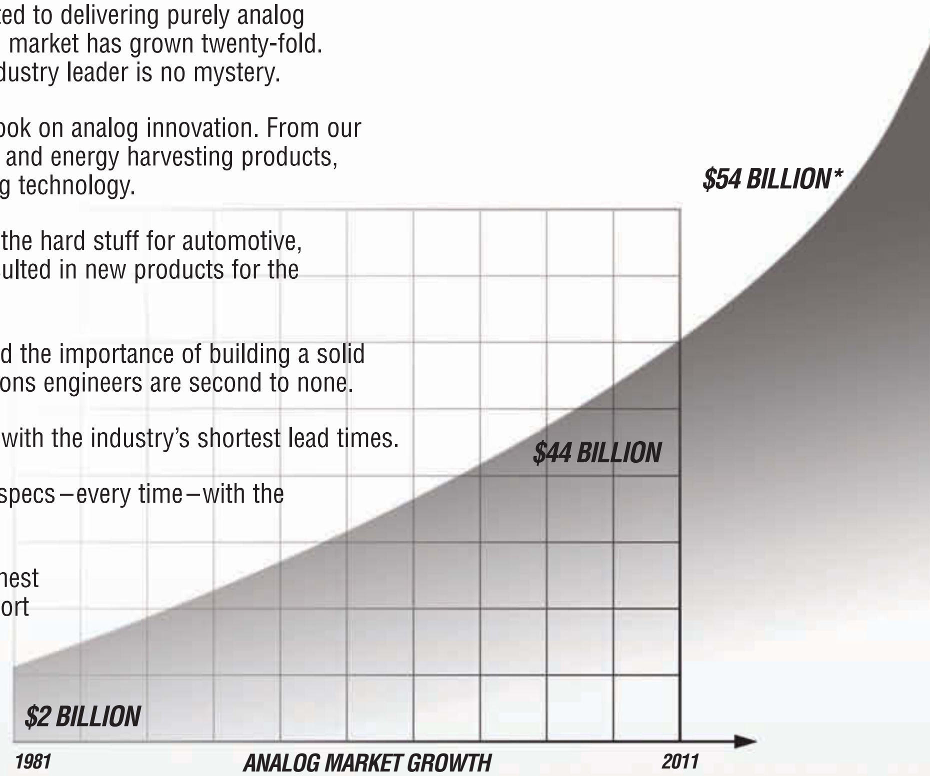

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